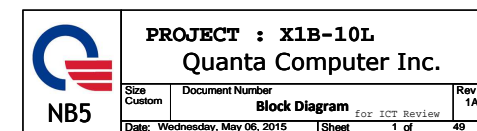


LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : SGND1
LAYER 7 : IN3
LAYER 8 : IN4
LAYER 9 : SGND2
LAYER 10 : BOT

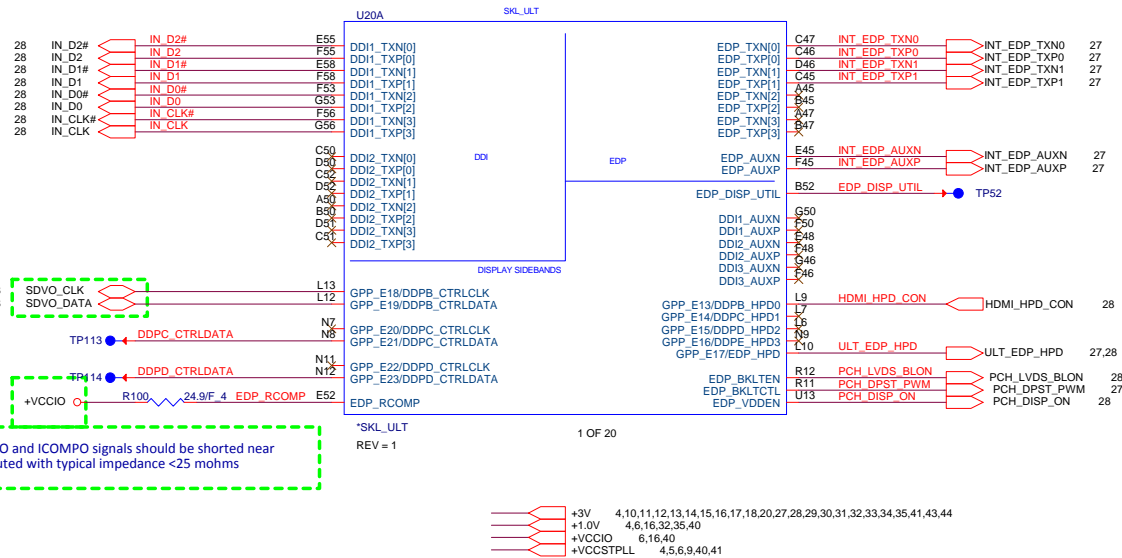


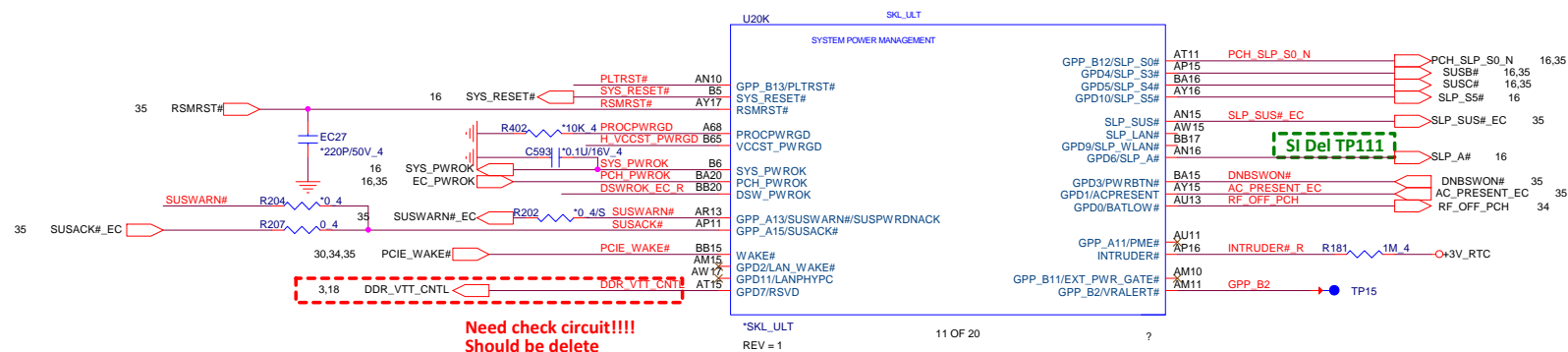
HDMI

DDPB_CTRLDATA/ GPP_E19
Display Port B Detected
This signal has a weak internal pull-down.
0 = Port B is not detected.
1 = Port B is detected.

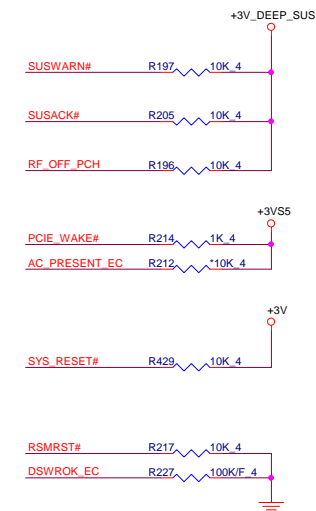
This signal has a weak internal pull-down.
0 = Port C and D is not detected.
1 = Port C and D is detected.

DB De1 R98, R110





PCH Pull-high/low(CLG)



+3V	2,10,11,12,13,14,15,16,17,18,20,27,28,29,30,31,32,33,34,35,41,43,44
+1.0V	2,6,16,32,35,40
+3V5S	10,15,16,32,34,35,37,39,40,43,46
+5V5S	30,32,33,37,38,39,40,41,42,43,44,45,46
+3V_RTC	13,15,32
+VCCSTPLL	2,5,6,9,40,41
+3V_DEEP_SUS	10,11,12,14,15,16,18

For DS3 Sequence

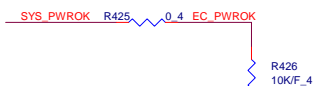


PLTRST#(CLG)

Check Q2010 Rise/Fall time less than 100ns

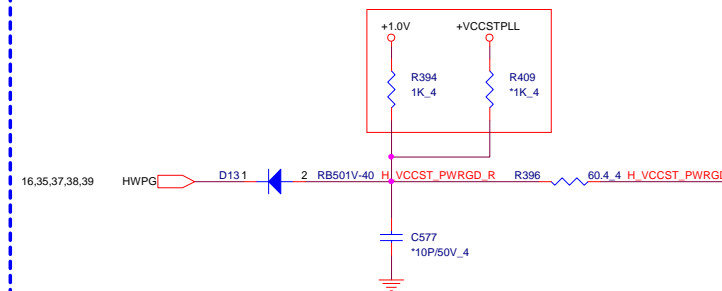


System PWR_OK(CLG)

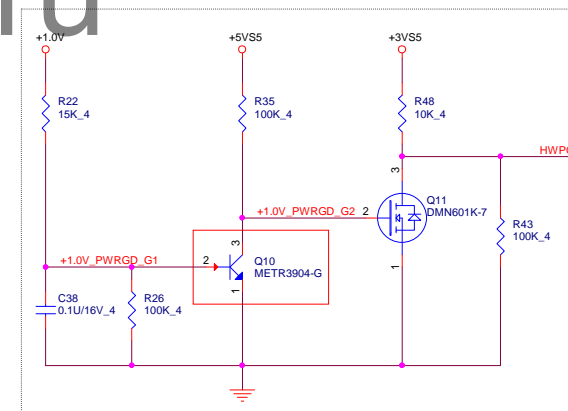


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1216 Change R409 and R394 from +VCCSTPLL or +1.0V co-layout.



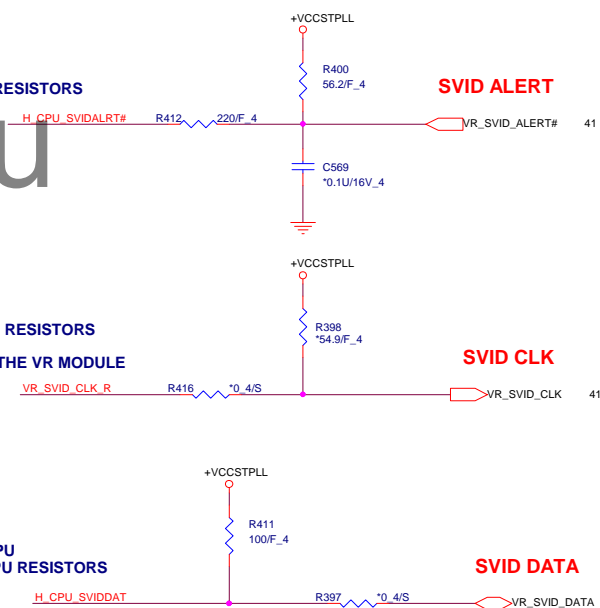
R10479 close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



1110 Add Citcuit for +1.0V Power Good



	+VCCSTG	6
	+VCCSTPLL	2,4,6,9,40,41
	+VCC CORE	41





IO Ther Protect

For 75 degree, 1.2v limit, (HW)

35

CHOCK Ther Protect

For 75 degree, 1.2v limit, (HW)

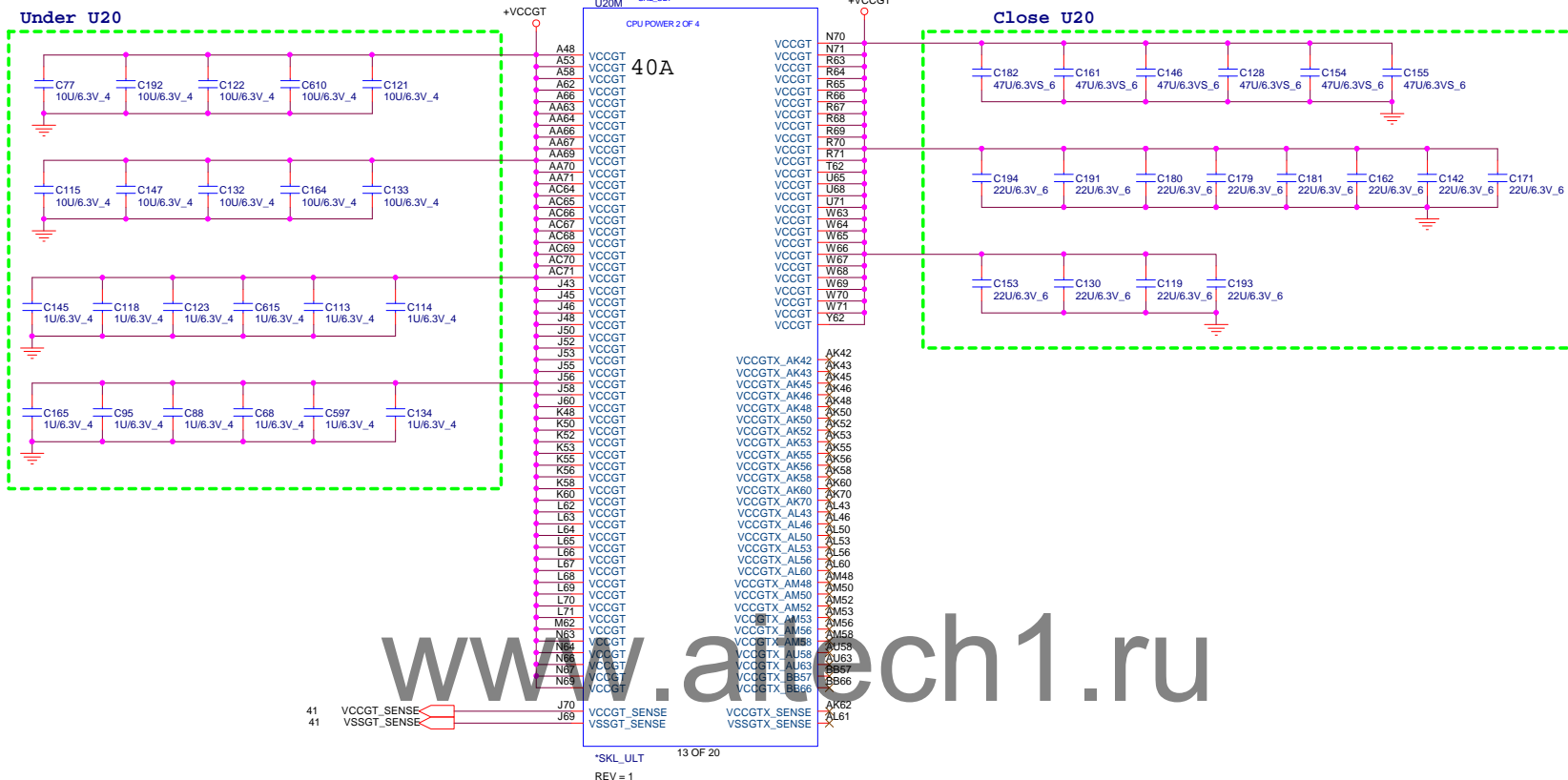
35

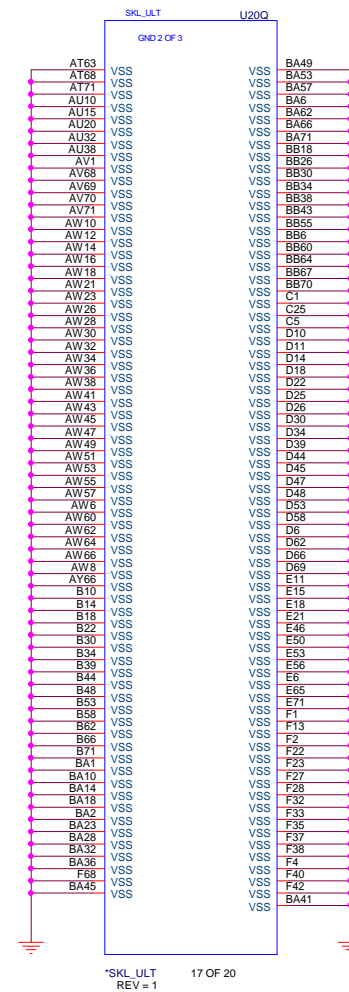
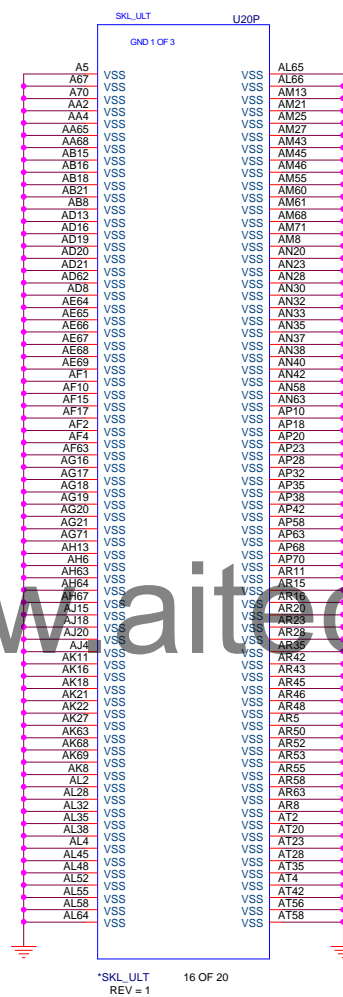
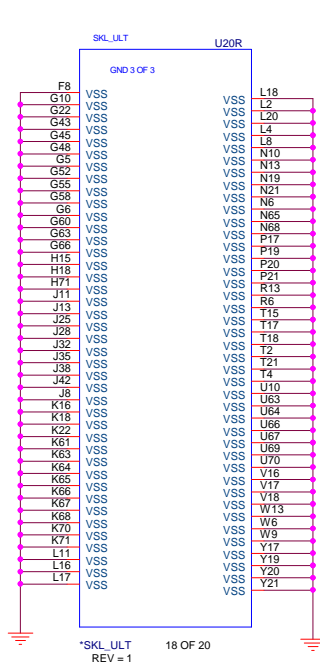
DDR Ther Protect

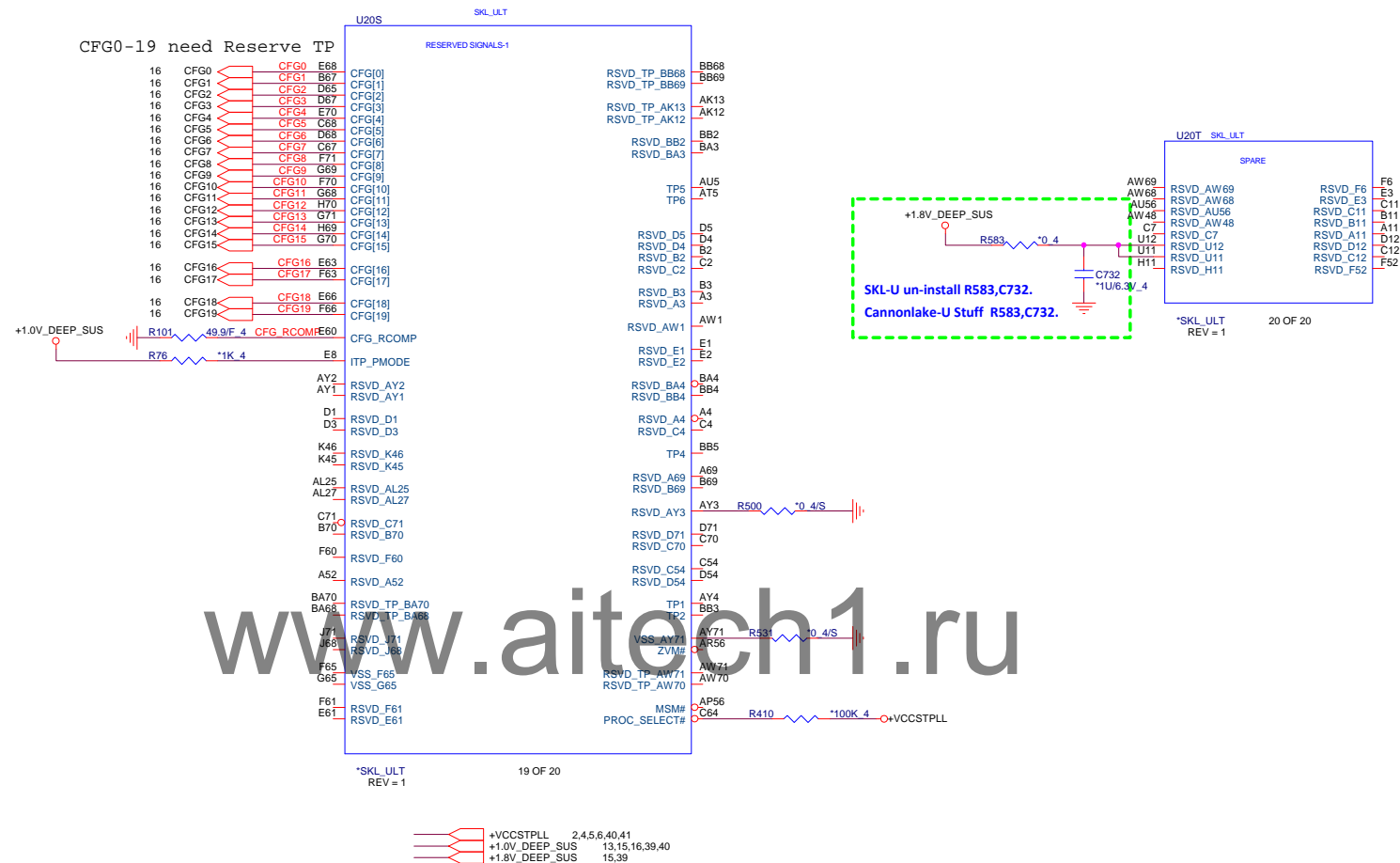
For 75 degree, 1.2v limit, (HW)

35

R579 Close to U15



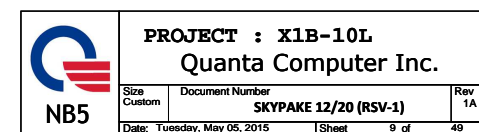


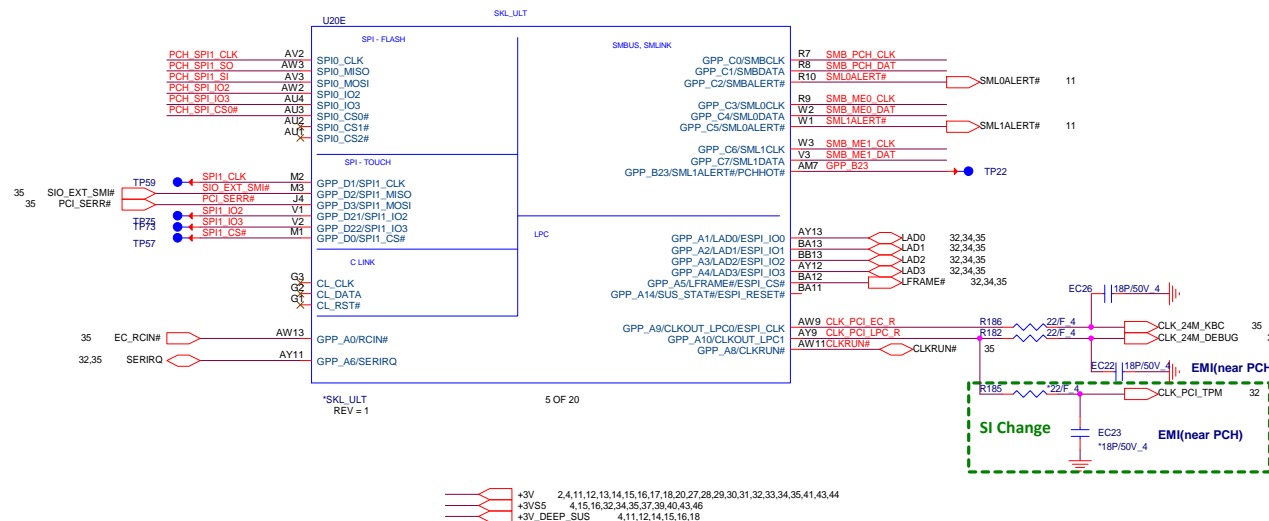


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

Processor Strapping			
	1	0	Circuit
CFG3 (Physical Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	





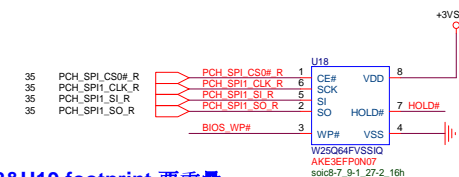
GPIO Pull UP



PCH SPI ROM(CLG)

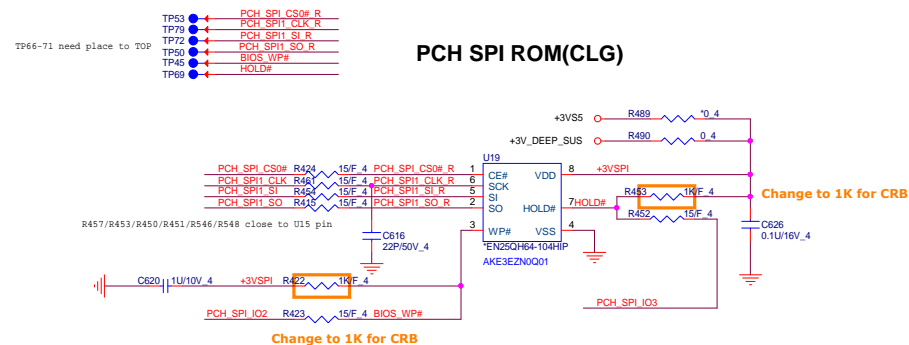
Vender	Size	P/N
EON	8MB	AKE3EZNOQ01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE2EZNOQ00 (GD25B64CSIGR)
Socket		DFHS08FS023 (HOUSING 8P 2R FS)

4M SPI ROM Socket

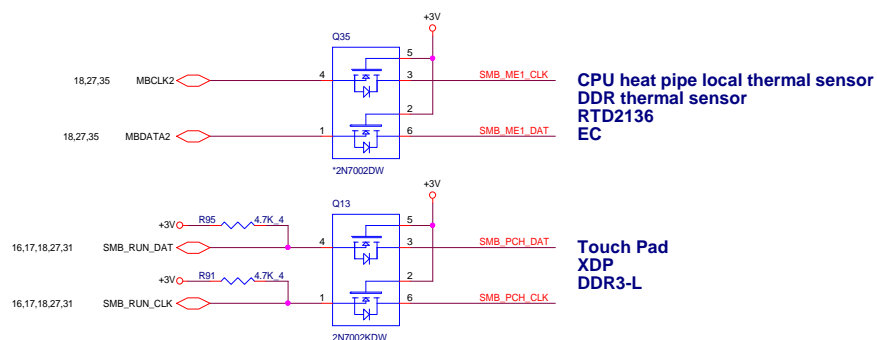


U18&U19 footprint 要重疊

PCH SPI ROM(CLG)



SMBus/Pull-up(CLG)

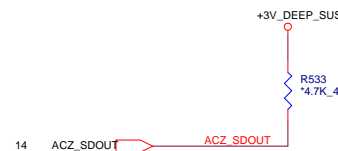


Functional Strap Definitions

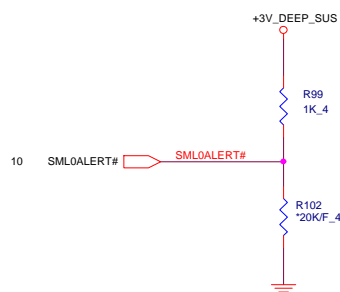
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



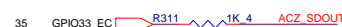
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD



No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



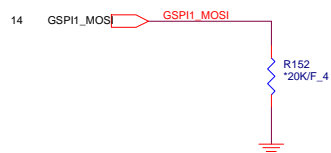
No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



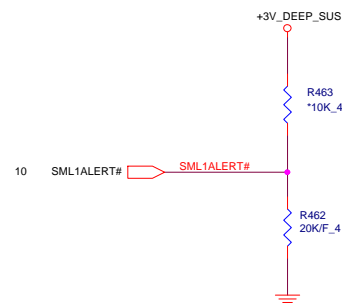
No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.



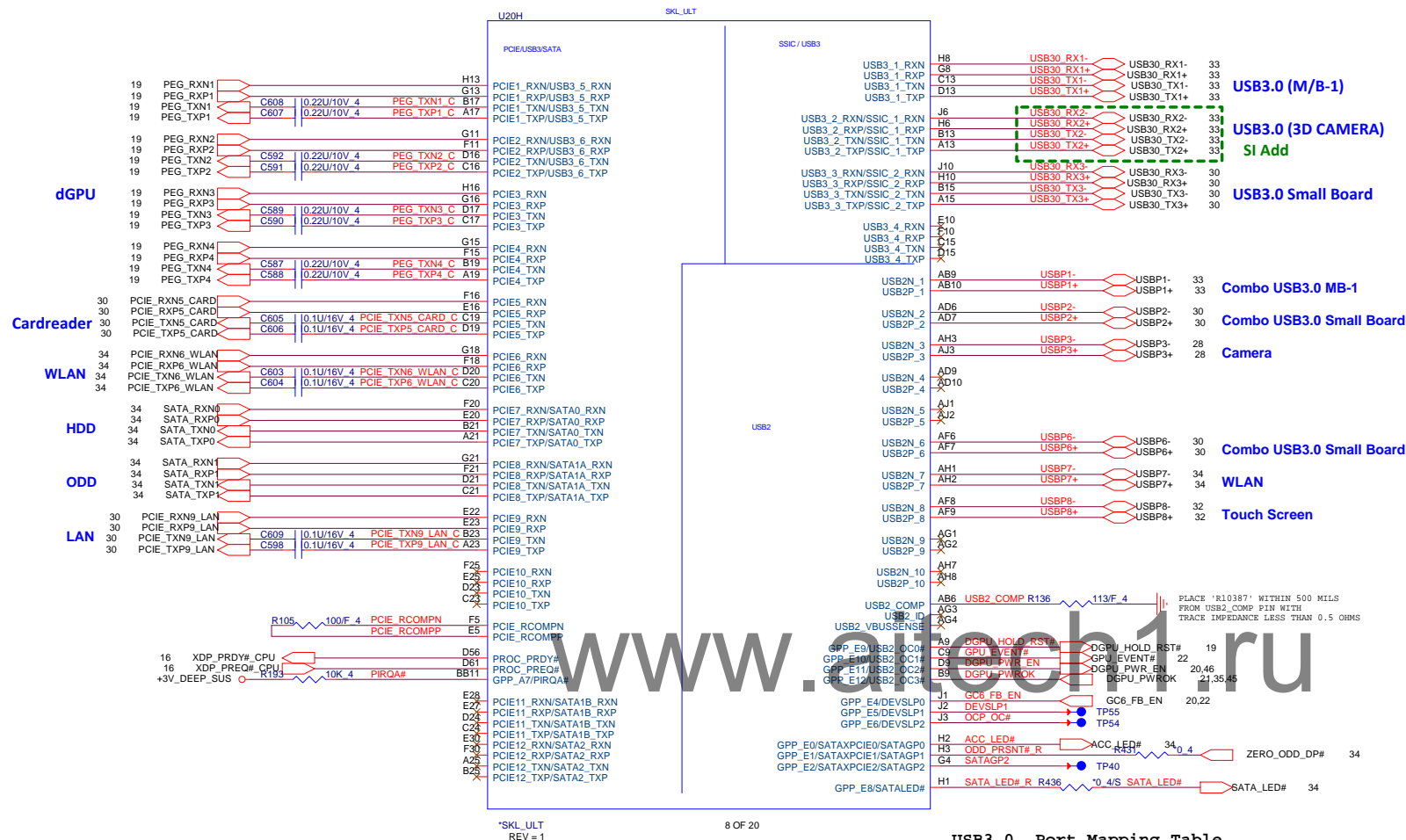
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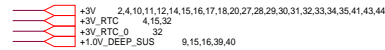
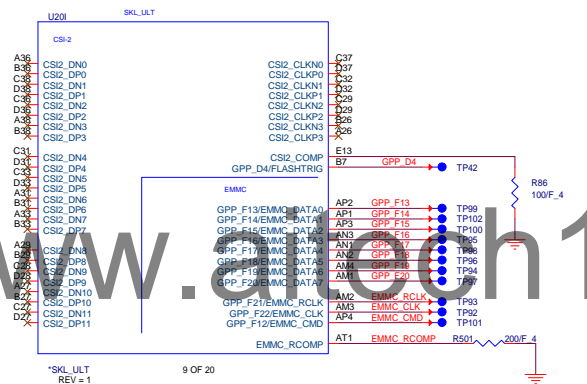
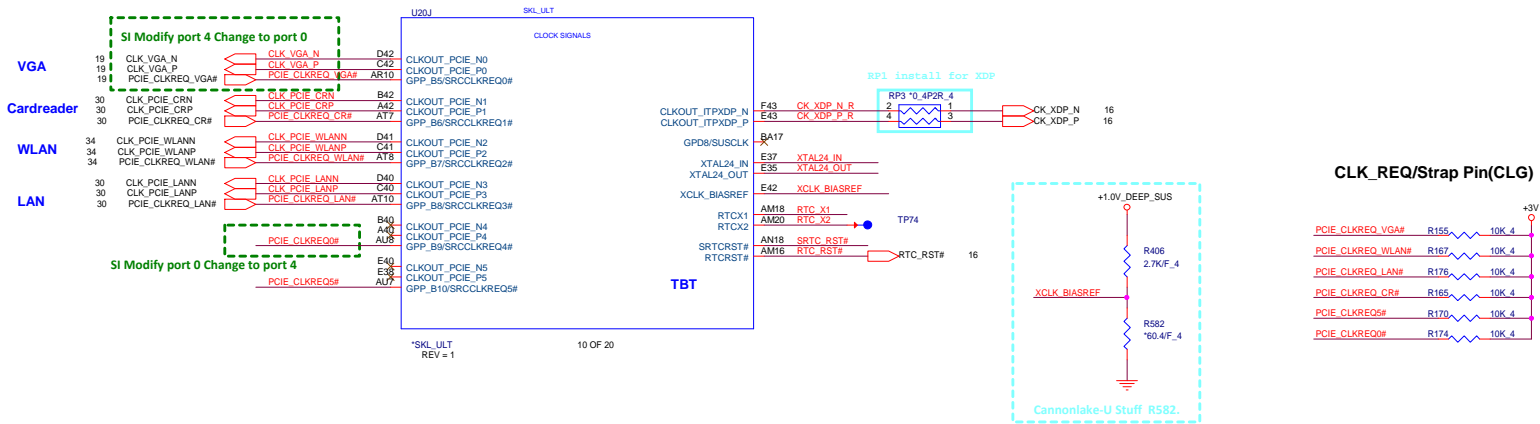


No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.
Bit 10 Boot BIOS Destination
0 SPI
1 LPC

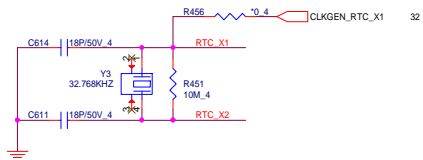


No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.

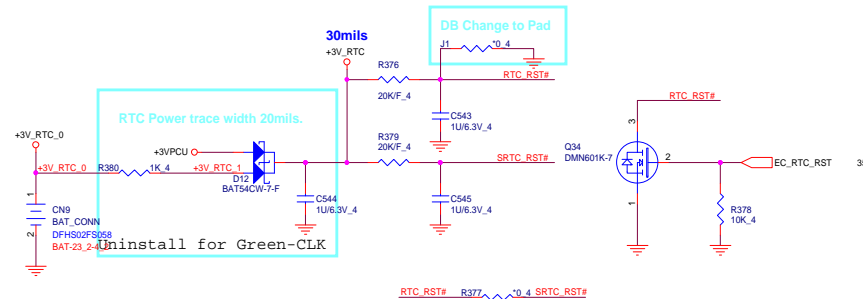




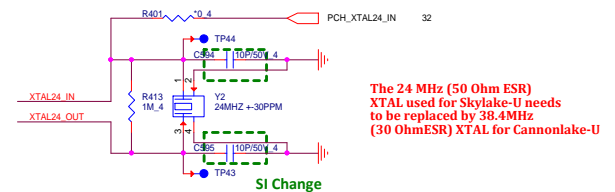
RTC Clock 32.768KHz

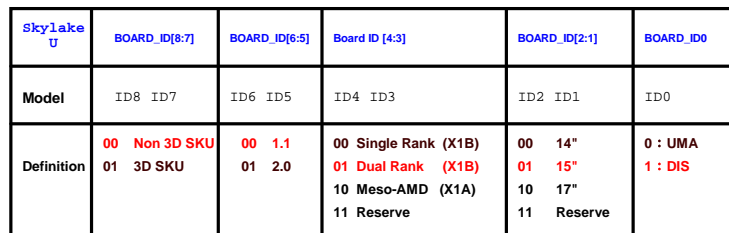


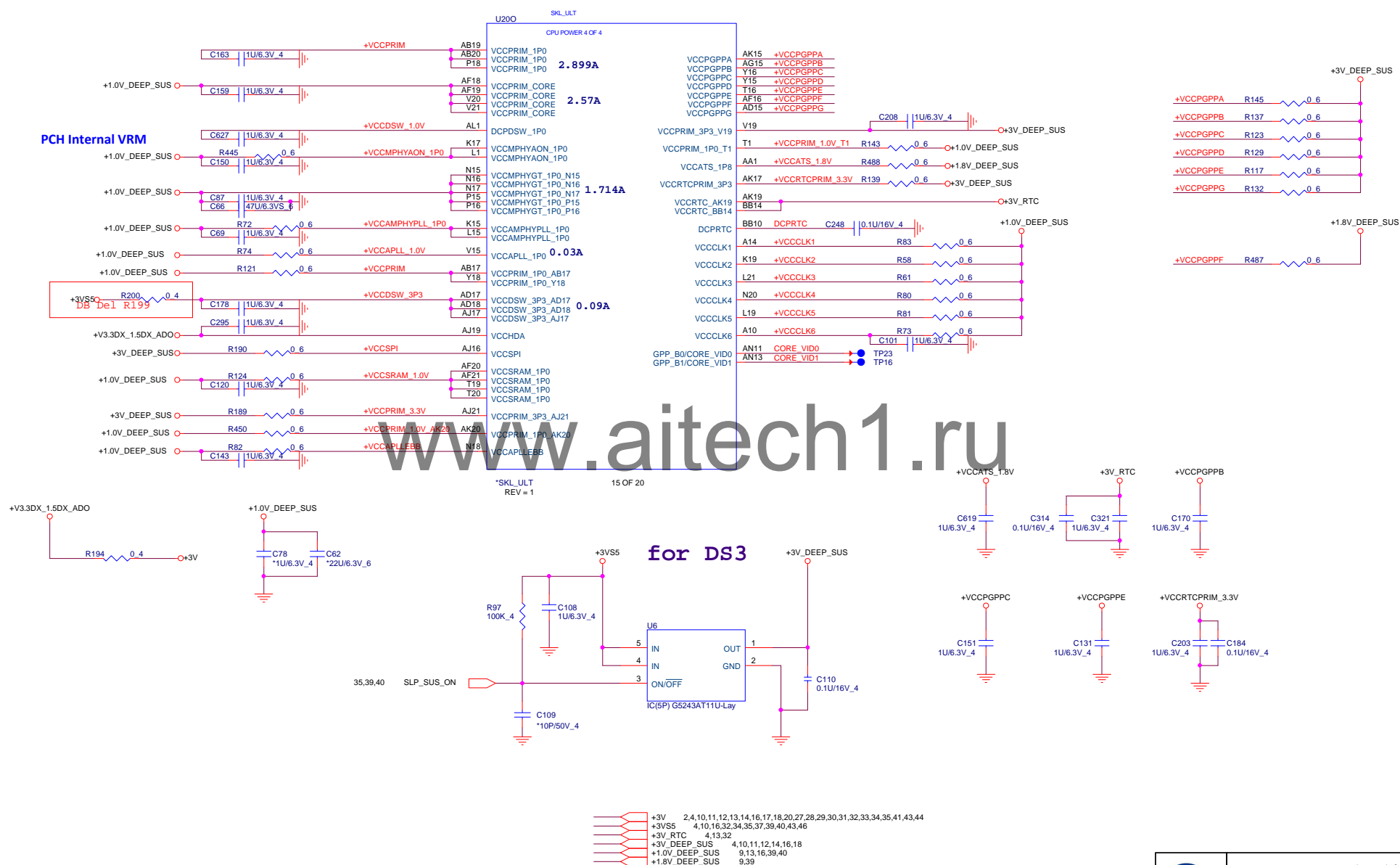
RTC Circuitry(RTC)



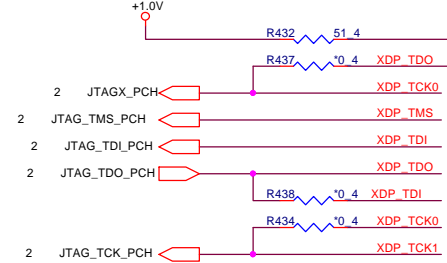
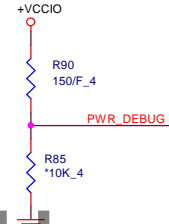
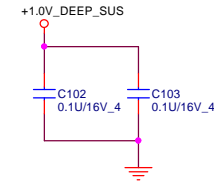
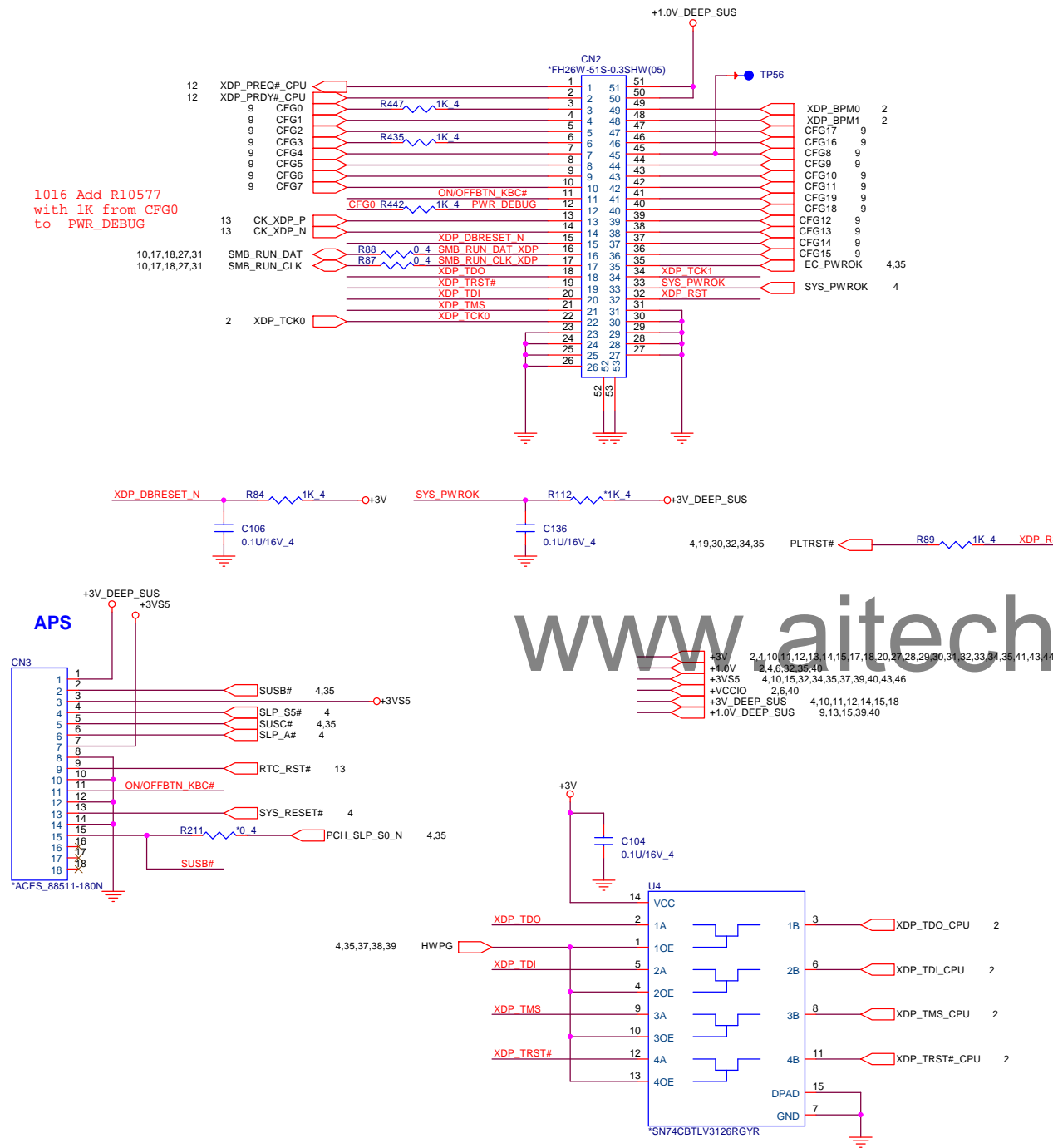
External Crystal and Green Clock





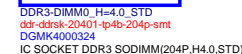
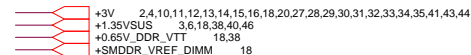


1016 Add R10577
with 1K from CFG0
to PWR_DEBUG



PROJECT : X1B-10L
Quanta Computer Inc.

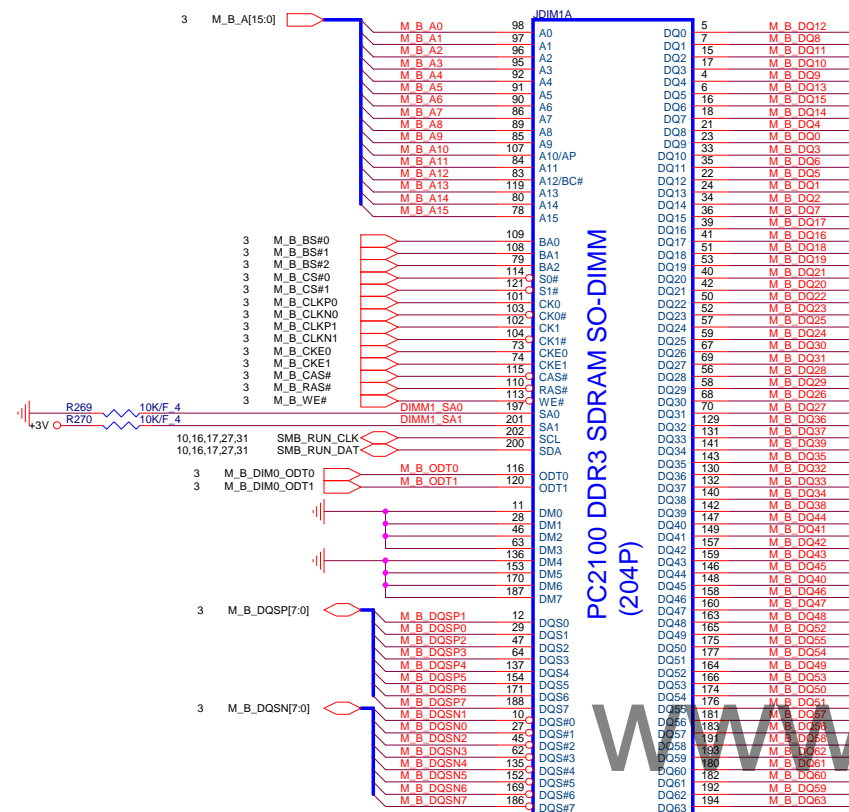
Size	Document Number	Rev
	HSW XDP & APS	1A
Date: Tuesday, May 05, 2015	Sheet 16 of 49	



M_B_DQ[63:0] 3

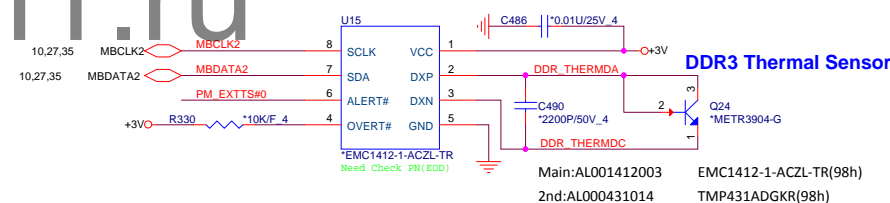
1006_Change group1 and group2 and DQ pins

+3V 2,4,10,11,12,13,14,15,16,17,20,27,28,29,30,31,32,33,34,35,41,43,44
 +1.35VSUS 3,6,17,38,40,46
 +3V_DEEP_SUS 4,10,11,12,14,15,16
 +0.65V_DDR_VTT 17,38
 +SMDRR_VREF_DIMM 17

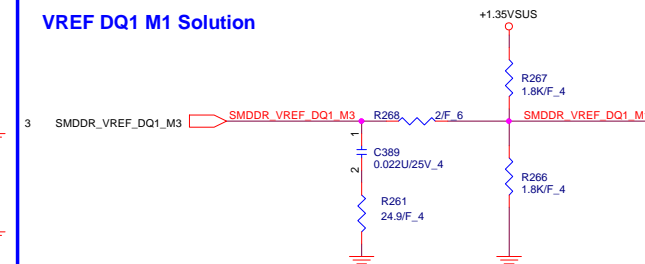


DDR3-DIMM1_H=4.0_RVS
 ddr-ddr3-20401-tp4b-204p-smt
 DGMK4000262

Local Thermal Sensor

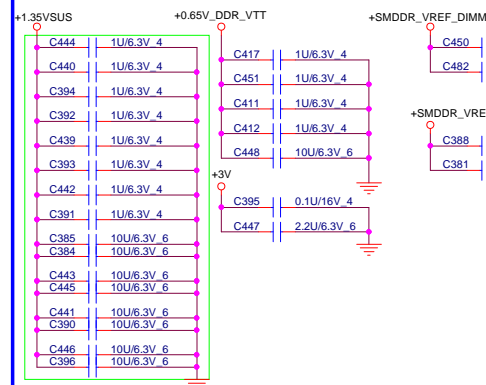
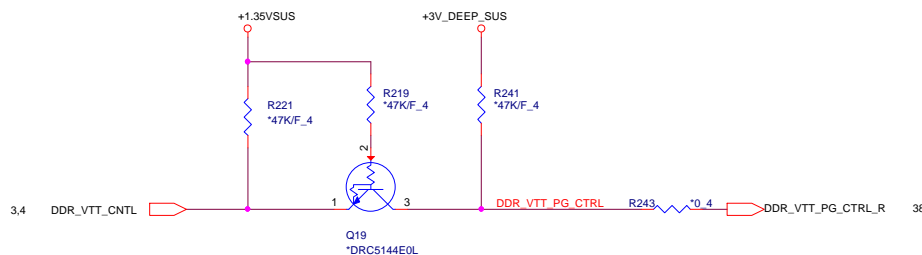


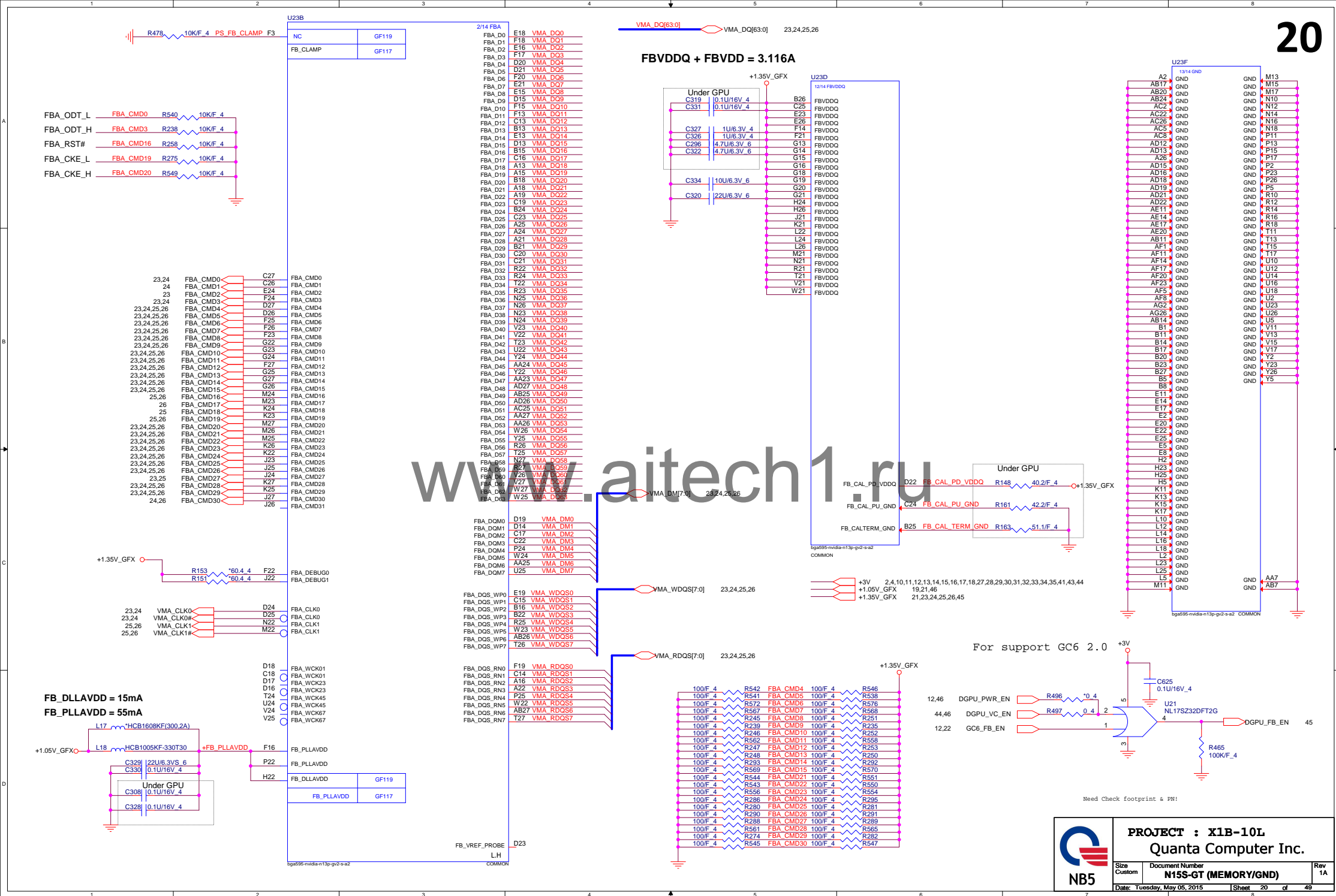
VREF DQ1 M1 Solution

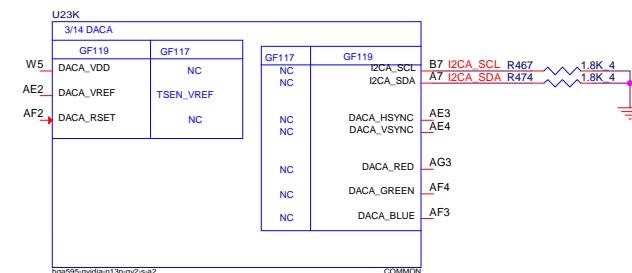
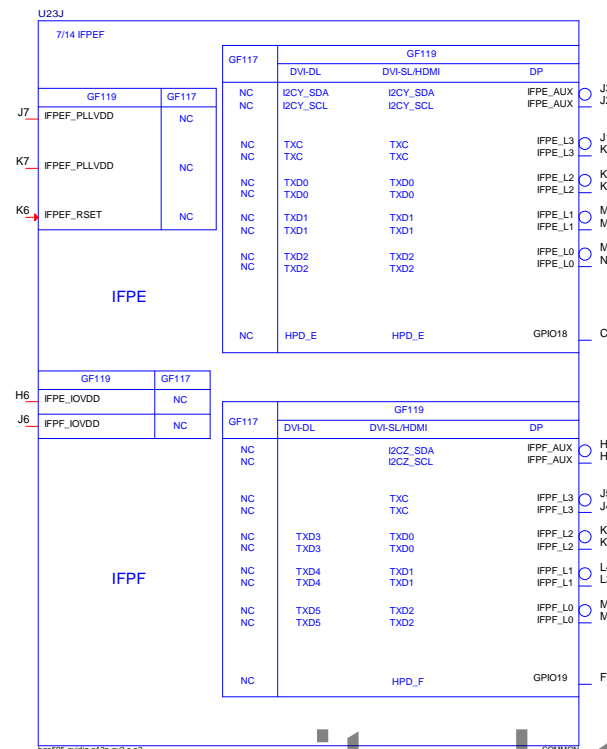
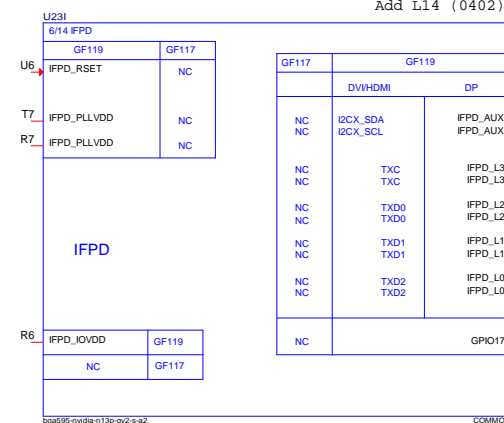
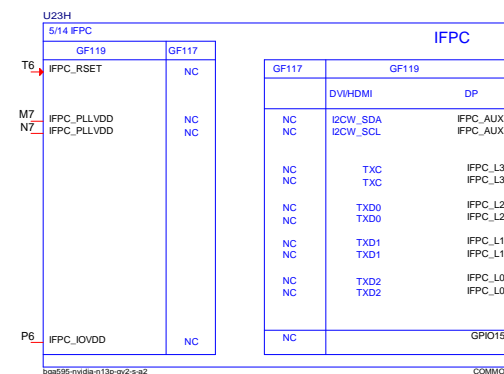
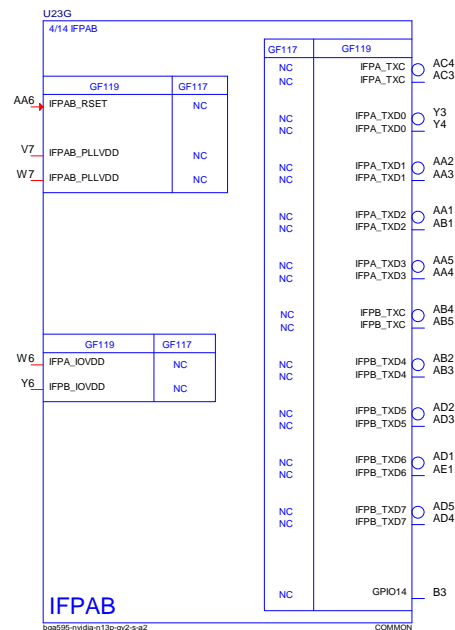


Place these Caps near So-Dimm1.

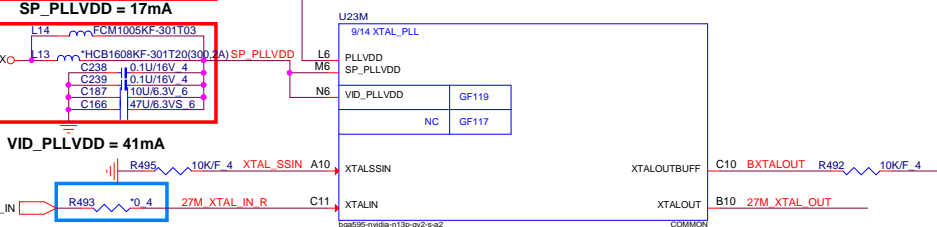
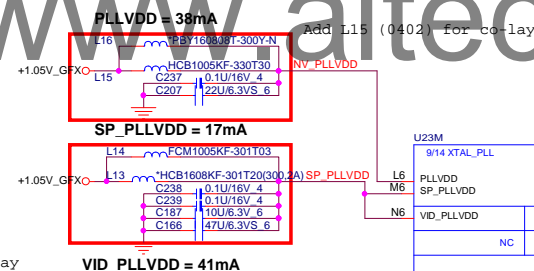
1uF/10uF 4pcs on each side of connector

Co-lay for ODT
From Intel MOW, ODT directly connection to CPU



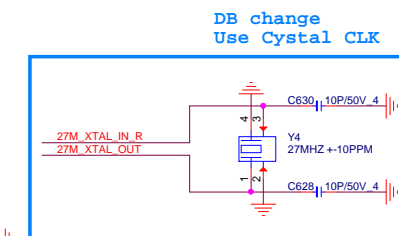
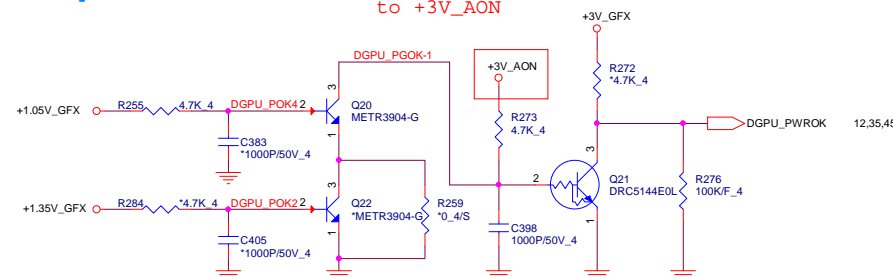


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DB change
Use Cystal CLK

1027 Change +3V
to +3V_AON



+3V_GFX	19,22,44,46
+3V_AON	19,22,32,46
+1.05V_GFX	19,20,46
+1.35V_GFX	20,23,24,25,26,45

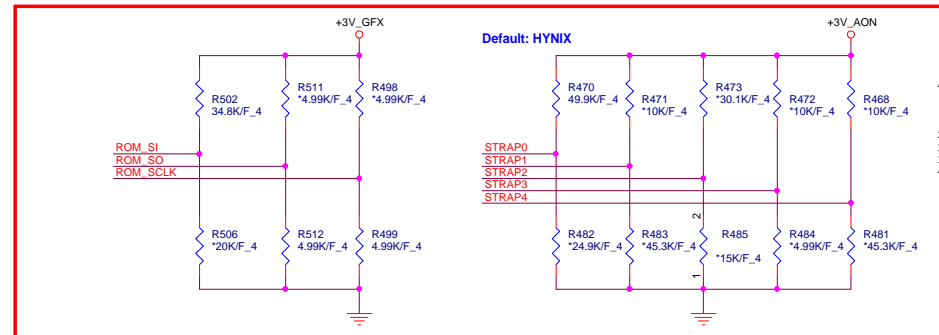
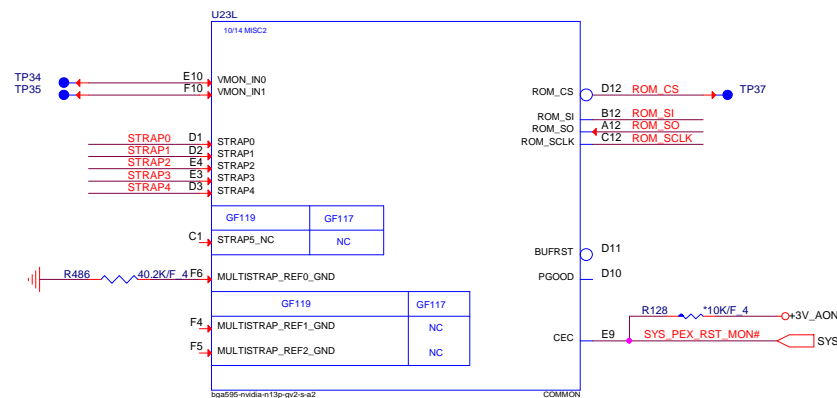
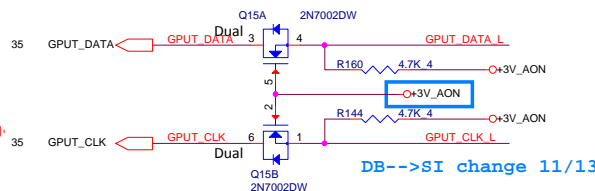
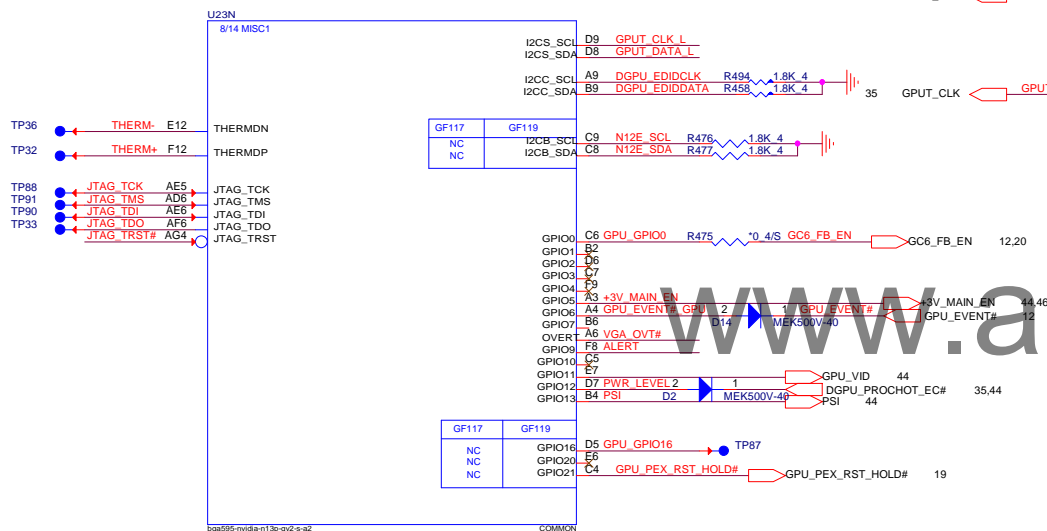


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111



VRAM Configuration Table

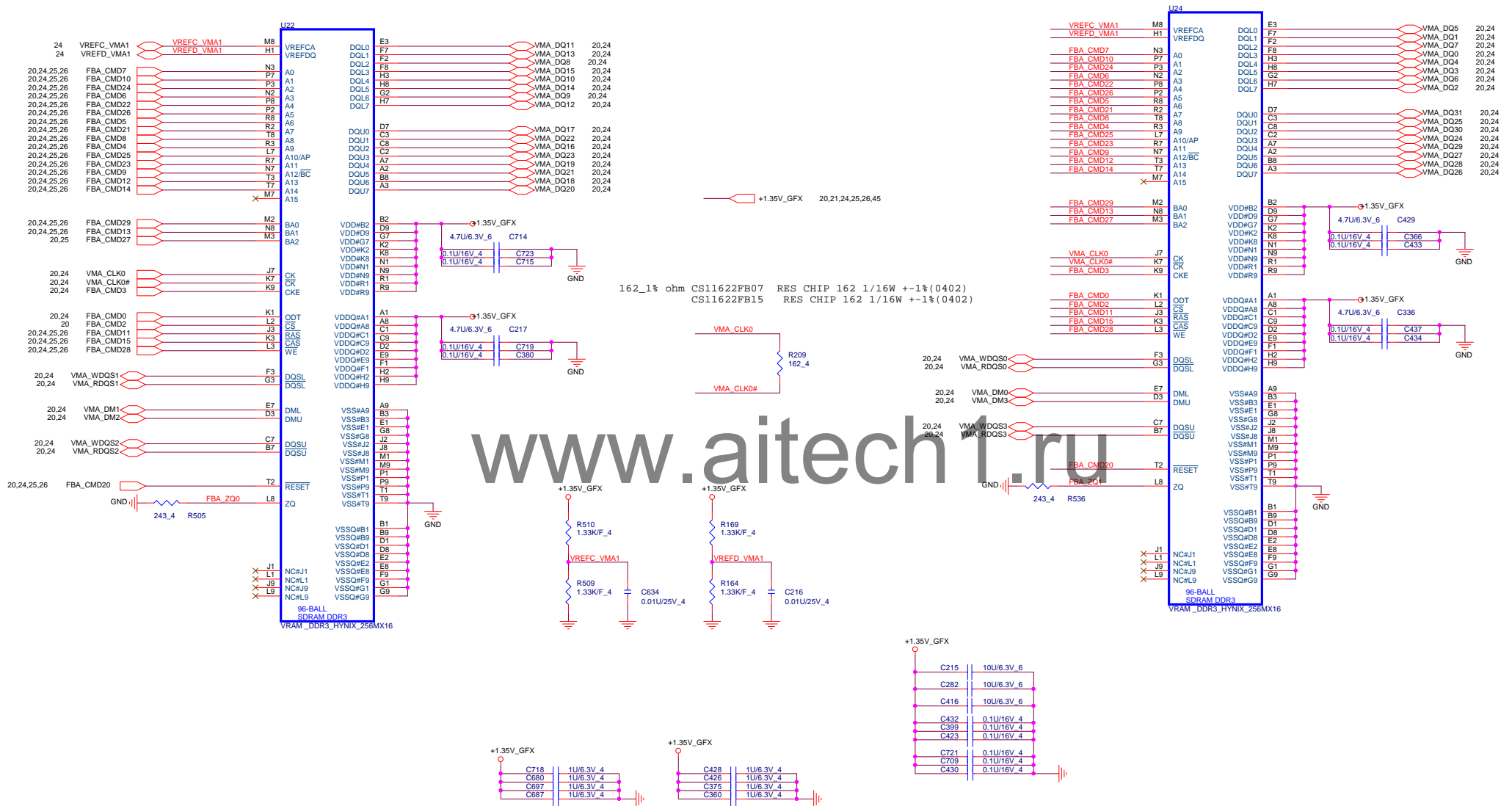
RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	256Mx16 Strap	128Mx16 Strap	QBC	TOP B/S
1110	DDR3L 256Mx16, 64bit, 4Gb, 900MHz	HYNIX	H5TC4G63CFR-N0C	0XE	TBD	AKD5PZDTW02	AKD5PZDTW01
0011	DDR3L 256Mx16, 64bit, 4Gb, 900MHz	Micron	MT41J256M16HA-093G:E	0x4	TBD	AKD5PZSTL01	AKD5PZSTL00
1111	DDR3L 256Mx16, 64bit, 4Gb, 900MHz	SAMSUNG	K4W4G1646E-BC1A	0XF	TBD	AKD5PGDT501	AKD5PGDT500

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMMORY_VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

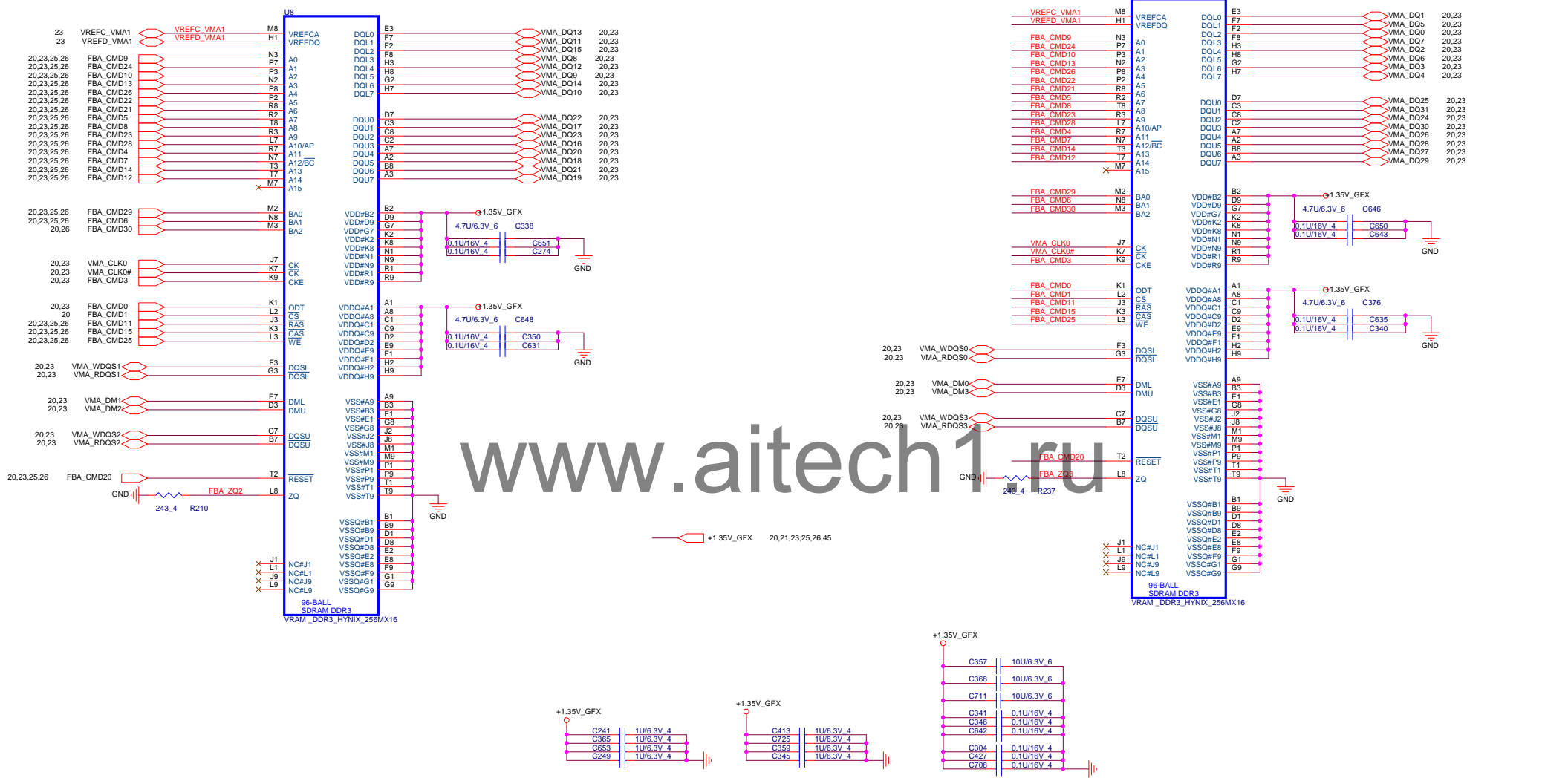
Rank0

HYU 256Mx16, H5TC4G63CFR-N0C QBC PN : AKD5PZDTW02---TOP B/S PN : AKD5PZDTW01
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Mx16, K4W4G1646E-BC1A QBC PN : AKD5PGDT501---TOP B/S PN : AKD5PGDT500



Rank1

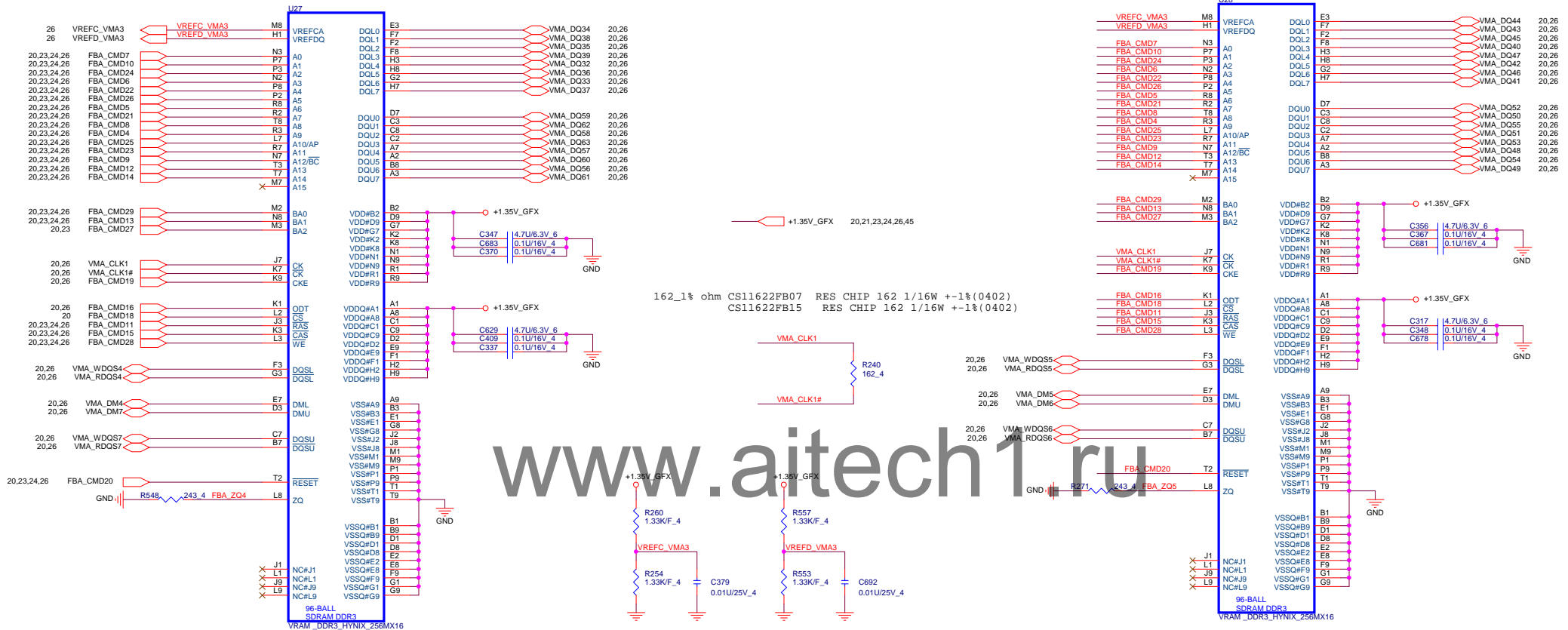
HYU 256Mx16, H5TC4G63CFR-N0C QBC PN : AKD5PZDTW02---TOP B/S PN : AKD5PZDTW01
 MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
 SAM 256Mx16, K4W4G1646E-BC1A QBC PN : AKD5PGDT501---TOP B/S PN : AKD5PGDT500



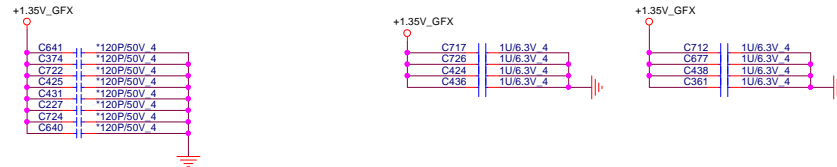
Rank0

HYU 256Mx16, H5TC4G63CFR-N0C
 MIC 256Mx16, MT41J256M16HA-093G:B
 SAM 256Mx16, K4W4G1646E-BC1A

QBC PN : AKD5PZDTW02---TOP B/S PN : AKD5PZDTW01
 QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
 QBC PN : AKD5PGDT501---TOP B/S PN : AKD5PGDT500

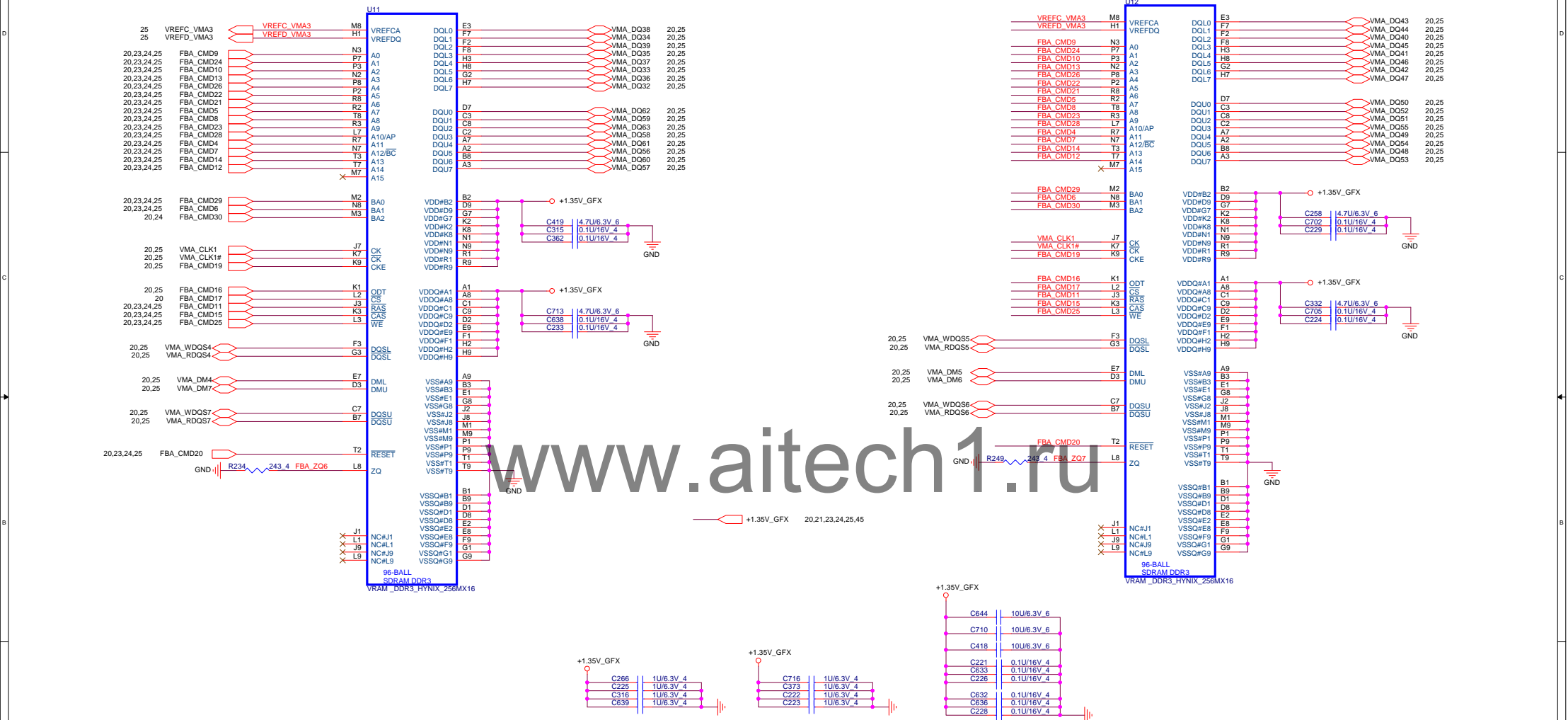


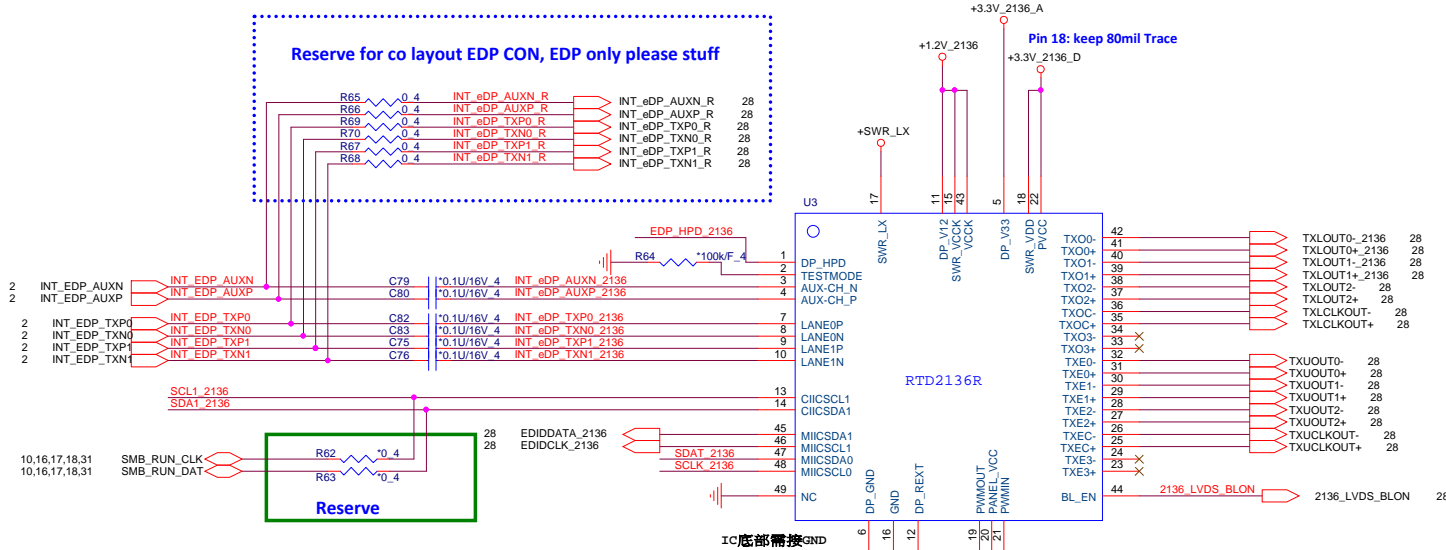
FOR EMI Request



Rank1

HYU 256Mx16, H5TC4G63CFR-N0C QBC PN : AKD5PZDTW02---TOP B/S PN : AKD5PZDTW01
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Mx16, K4W4G1646E-BC1A QBC PN : AKD5PGDT501---TOP B/S PN : AKD5PGDT500





EDDID EEPROM
VCC

DP2LVDS VCC

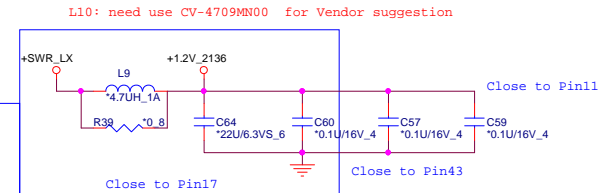
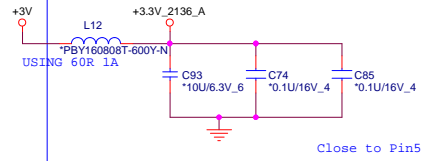
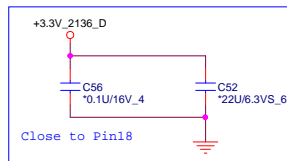
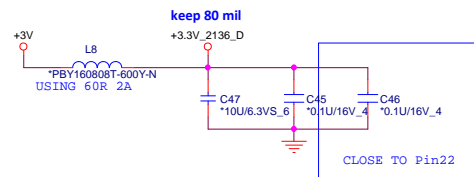
HPD

<=100ms

Default(LVDS Only)

For eDP, close to U3

LVDS Only



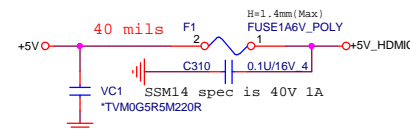
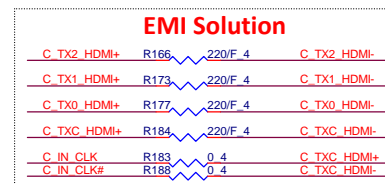
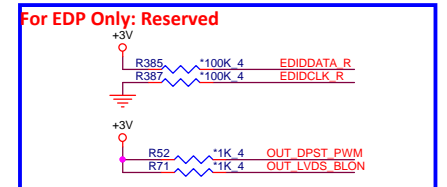
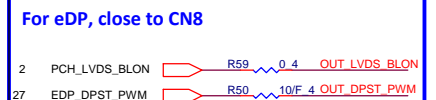
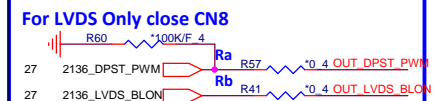
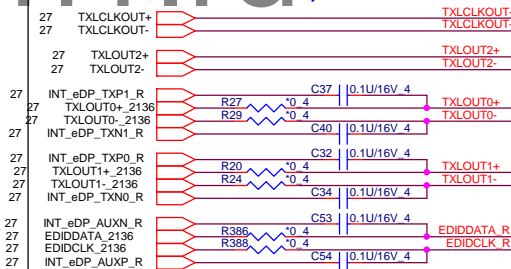
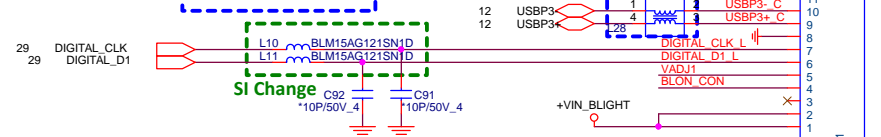
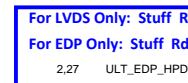
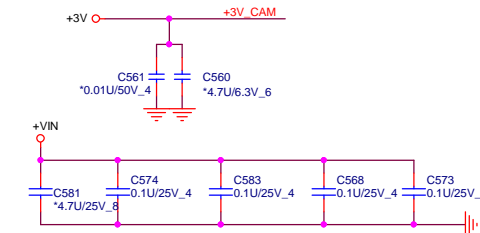
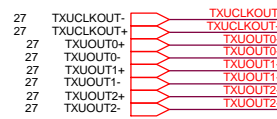
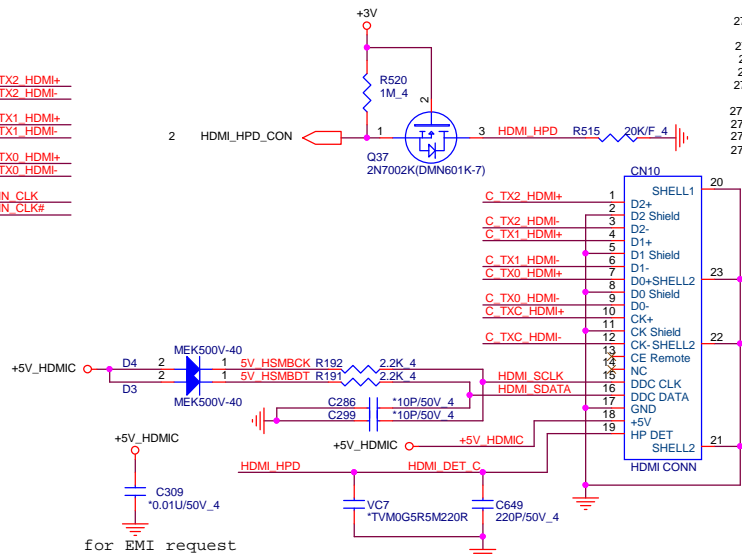
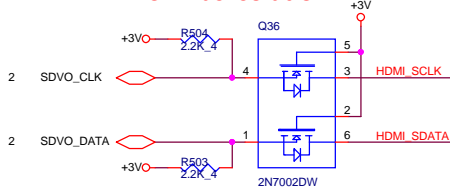
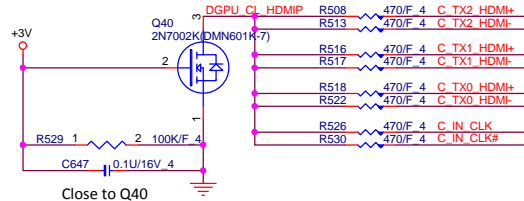
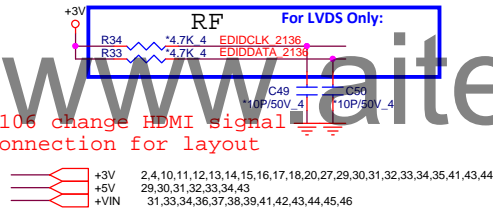
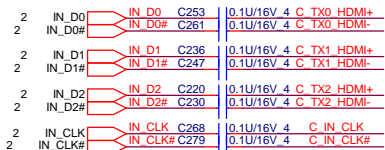
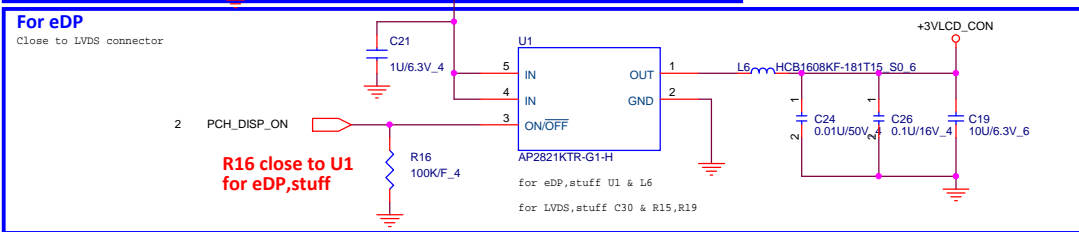
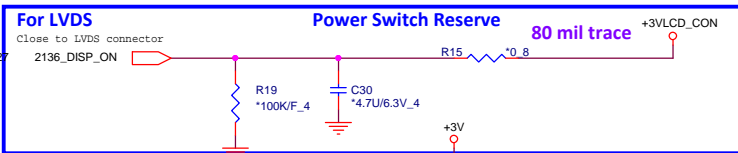
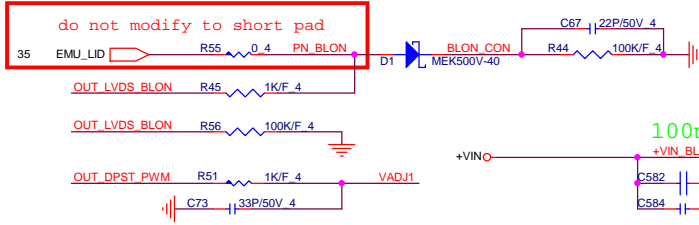
SWR MODE	LDO MODE
Stuff L9	Stuff R39

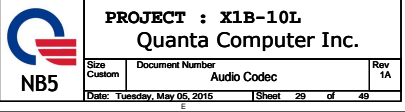


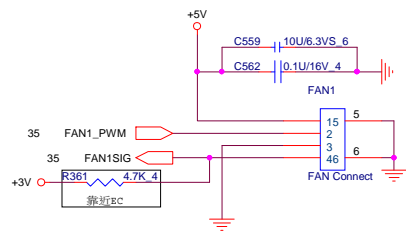
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Quanta Computer Inc.

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LID Switch

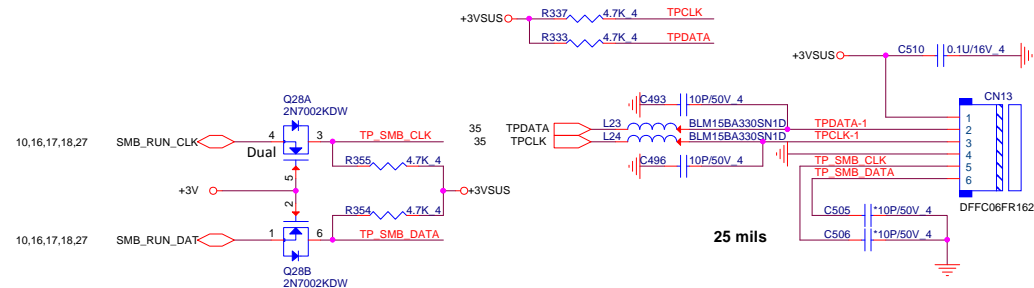






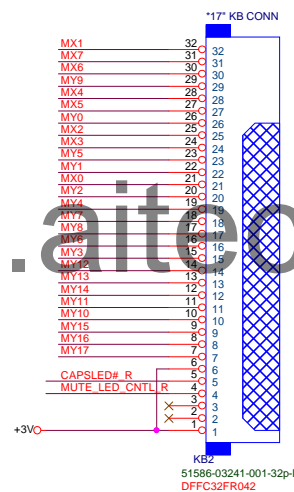
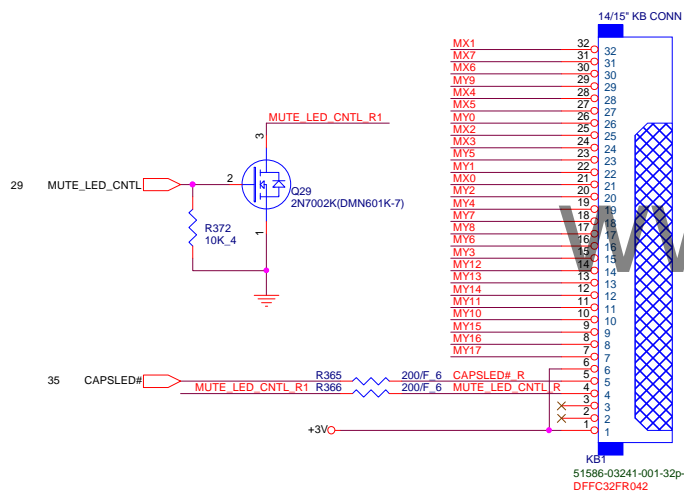
FAN1_PWM C565 *220P/50V_4
FAN1SIG C567 *220P/50V_4

+3V 2,4,10,11,12,13,14,15,16,17,18,20,27,28,29,30,32,33,34,35,41,43,44
+VIN 28,29,30,32,33,34,43
+3VSUS 33,43
+3VPCU 6,13,30,32,33,34,35,36,37

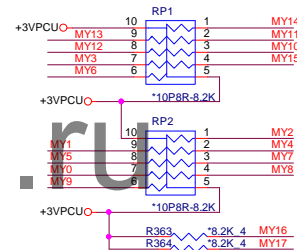


KEYBOARD Con.

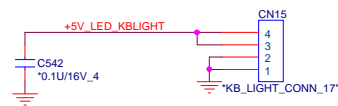
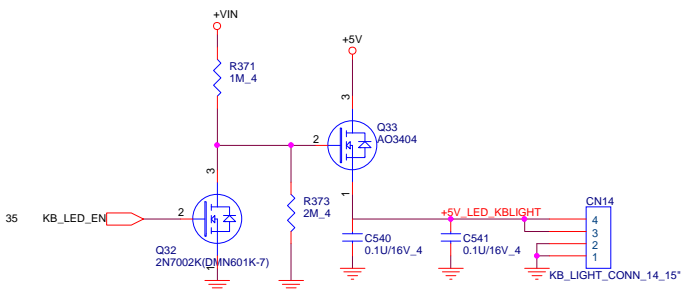
35 MY[0..17] MY[0..17]
35 MX[0..7] MX[0..7]



KEYBOARD PULL-UP



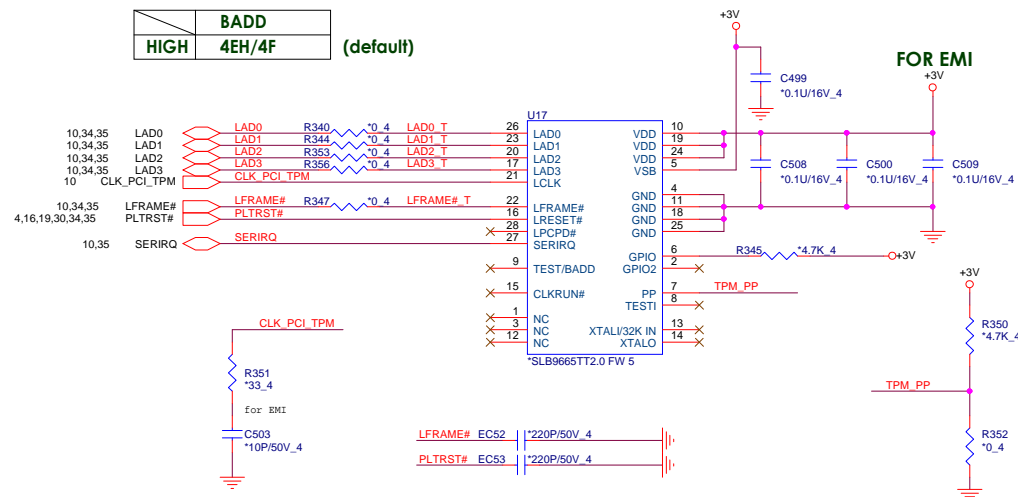
MY5 C523 *220P/50V_4
MY6 C530 *220P/50V_4
MY3 C531 *220P/50V_4
MY7 C528 *220P/50V_4
MY8 C529 *220P/50V_4
MY9 C517 *220P/50V_4
MY10 C536 *220P/50V_4
MY11 C535 *220P/50V_4
MY1 C524 *220P/50V_4
MY2 C526 *220P/50V_4
MY4 C527 *220P/50V_4
MY0 C520 *220P/50V_4
MX4 C518 *220P/50V_4
MX6 C516 *220P/50V_4
MX3 C522 *220P/50V_4
MX2 C521 *220P/50V_4
MX7 C515 *220P/50V_4
MX0 C525 *220P/50V_4
MX5 C519 *220P/50V_4
MX1 C514 *220P/50V_4
MY12 C532 *220P/50V_4
MY13 C533 *220P/50V_4
MY14 C534 *220P/50V_4
MY15 C537 *220P/50V_4
MY16 C538 *220P/50V_4
MY17 C539 *220P/50V_4



TPM (2.0)

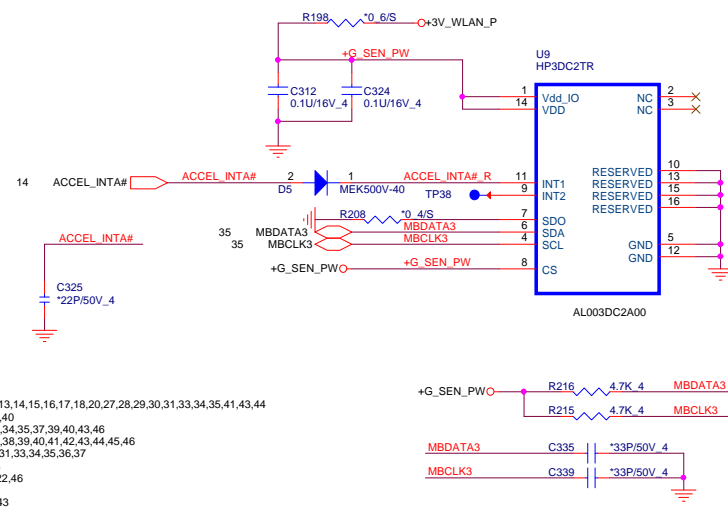
Address

	BADD
HIGH	4EH/4F (default)

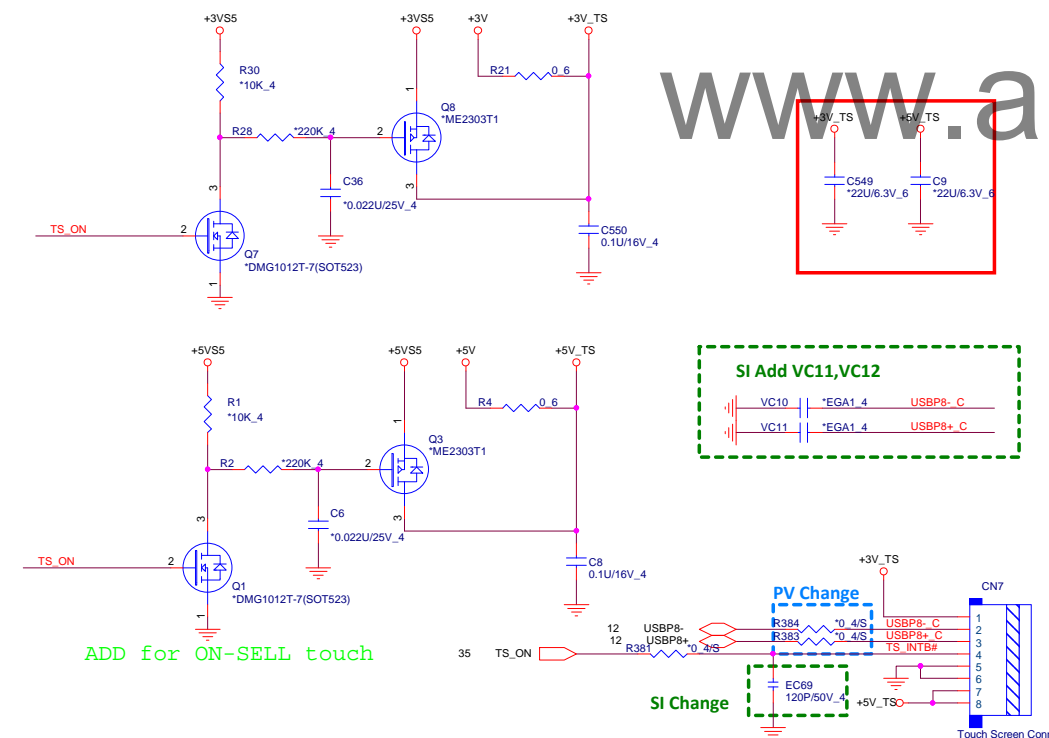


Accelerometer Sensor

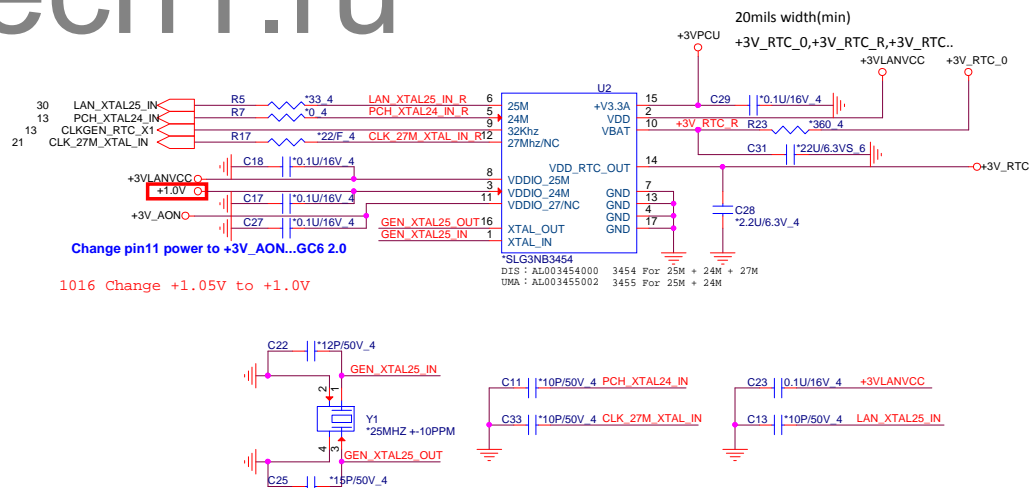
G-Sensor Power need check



Touch screen



Green CLK Circuitry



33

SI Add



3D Camera Conn.

SI Add 3D Camera Function



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non-USB 3.0 re-driver : stuff Ra



For Re-driver : stuff Ca



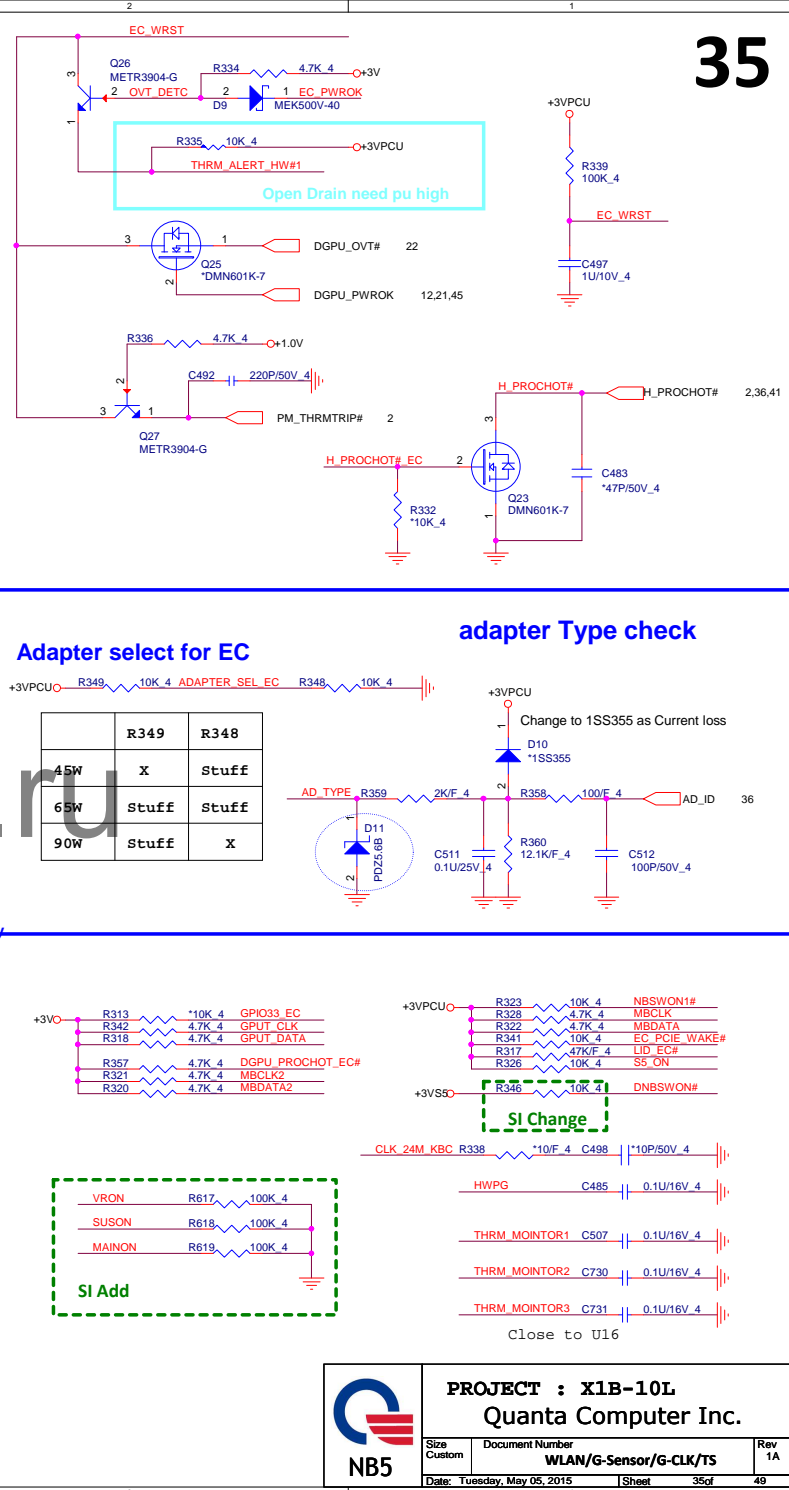
non-USB 3.0 re-driver : stuff Rb

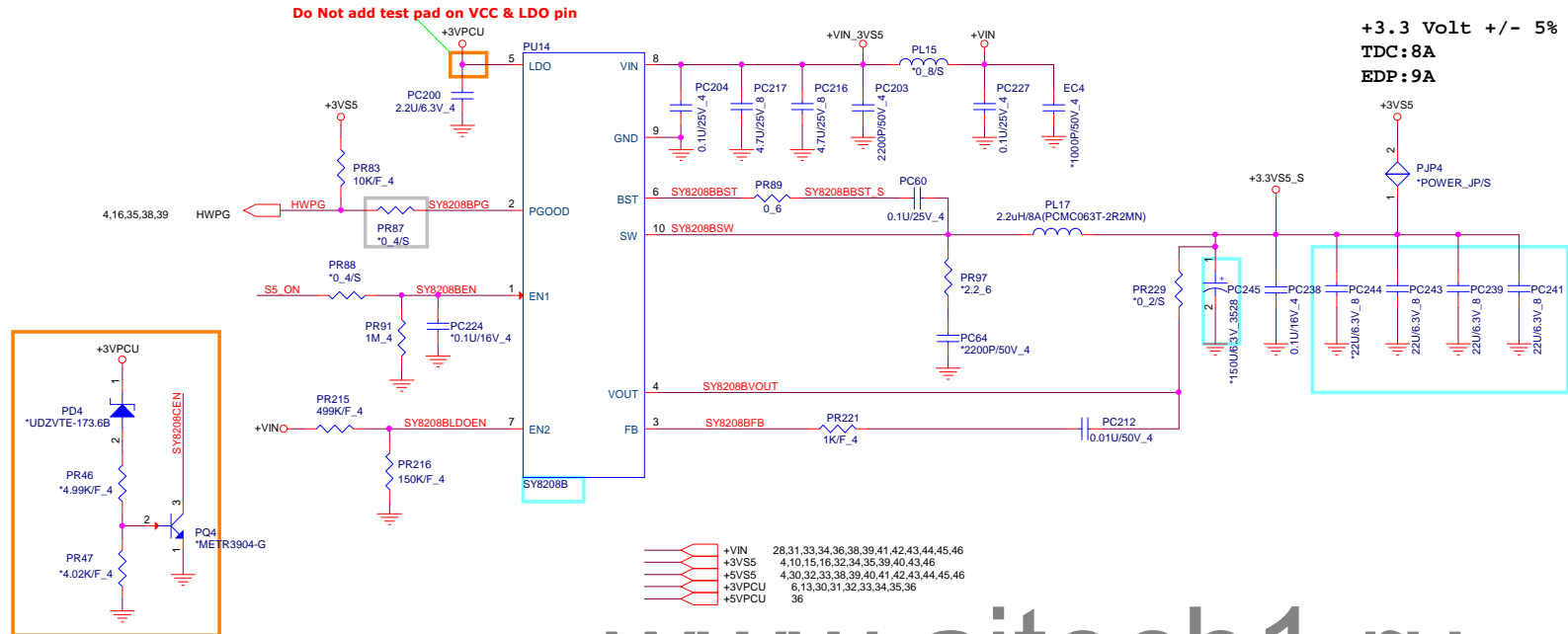


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Quanta Computer Inc.

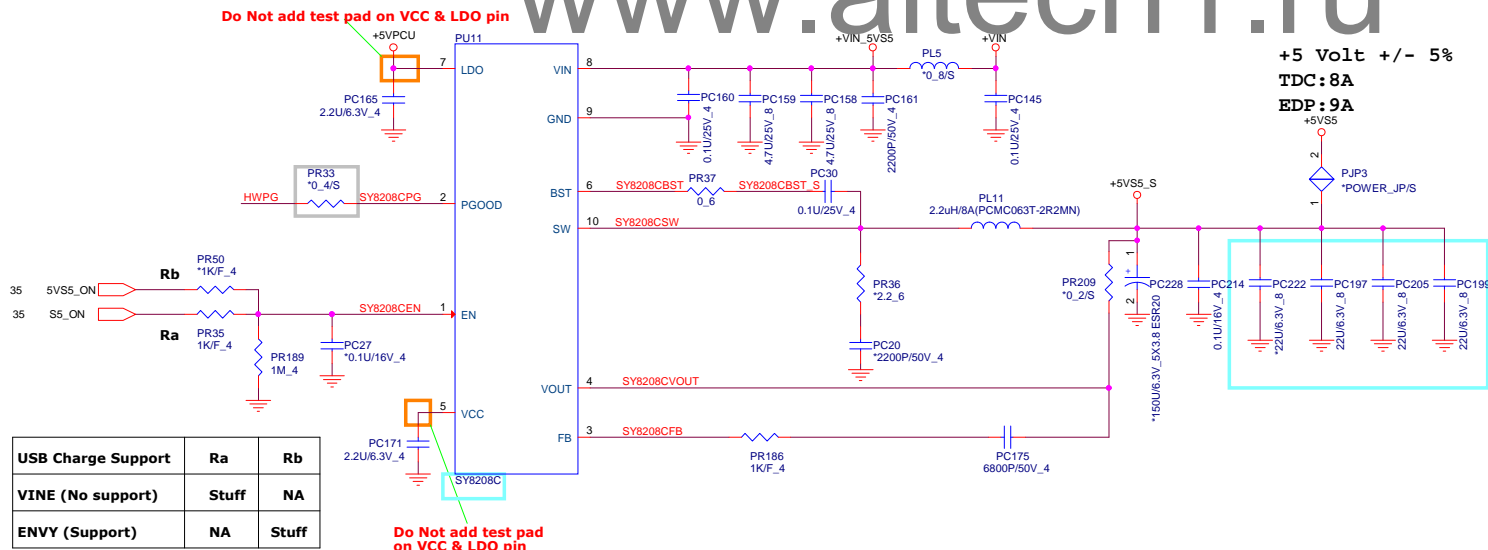
A_EQ1	A_EQ0		A_DE1	A_DE0	
B_EQ1	B_EQ0		B_DE1	B_DE0	
0	0	9.5dB	0	0	3.5dB
0	1	13dB	0	1	no de-emphasis
1	0	4.5dB	1	0	2.7dB
1	1	2.5dB	1	1	5dB

TST : Low = Normal LFPS swing / Hight =Turn down LFPS swing





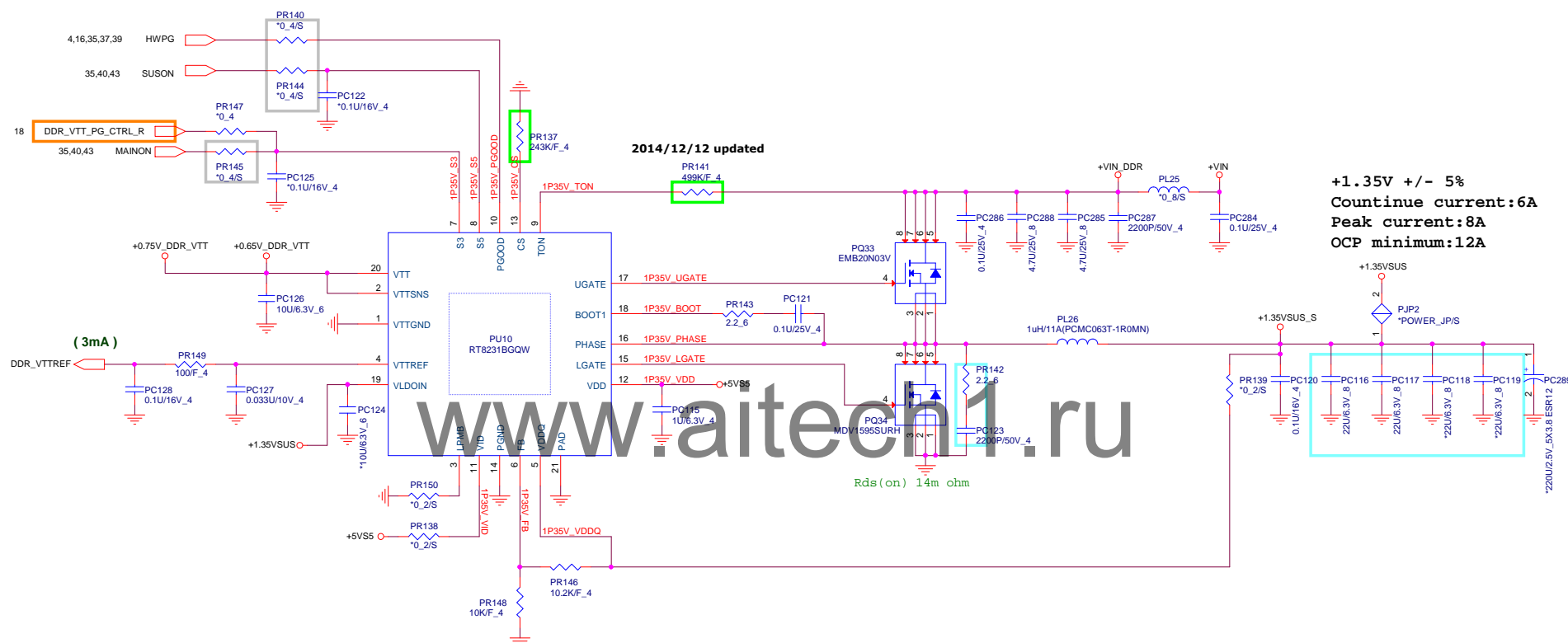
www.aitech1.ru

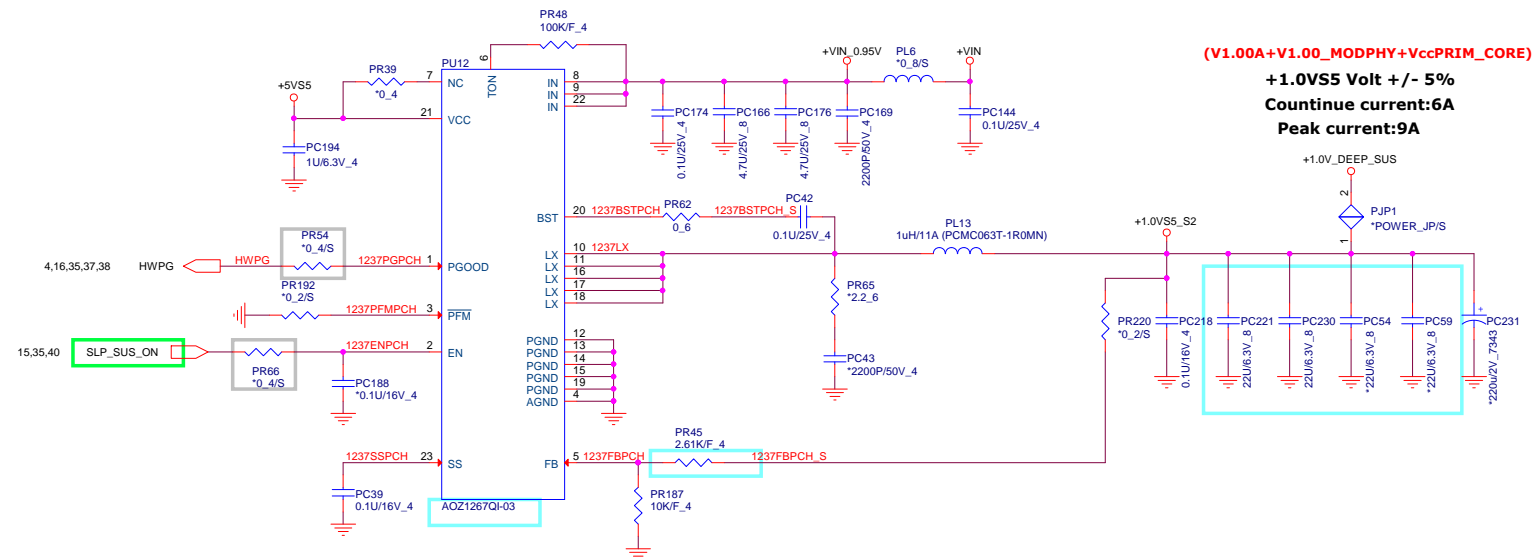


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Quanta Computer Inc.

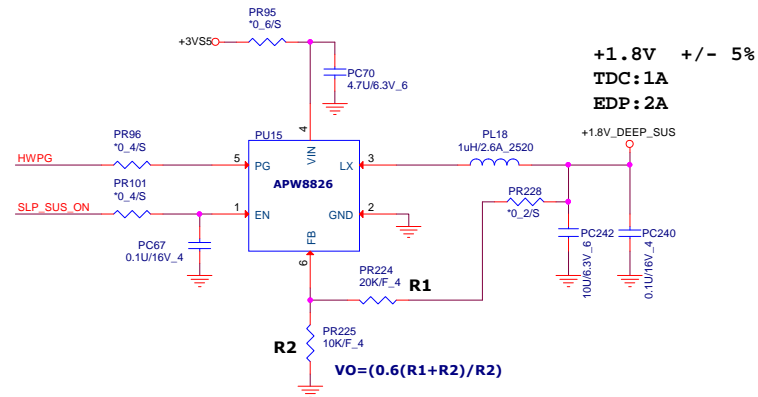
Size	Document Number	Rev
Custom	3/5VPCU(RT8243A)	1A

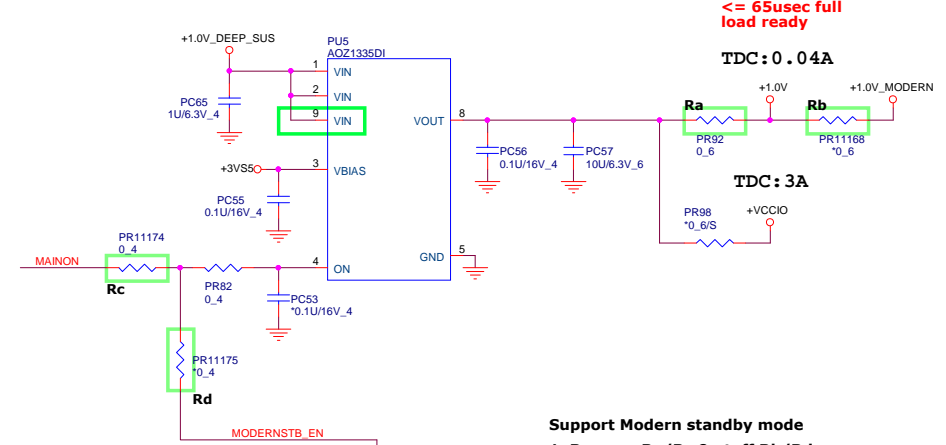
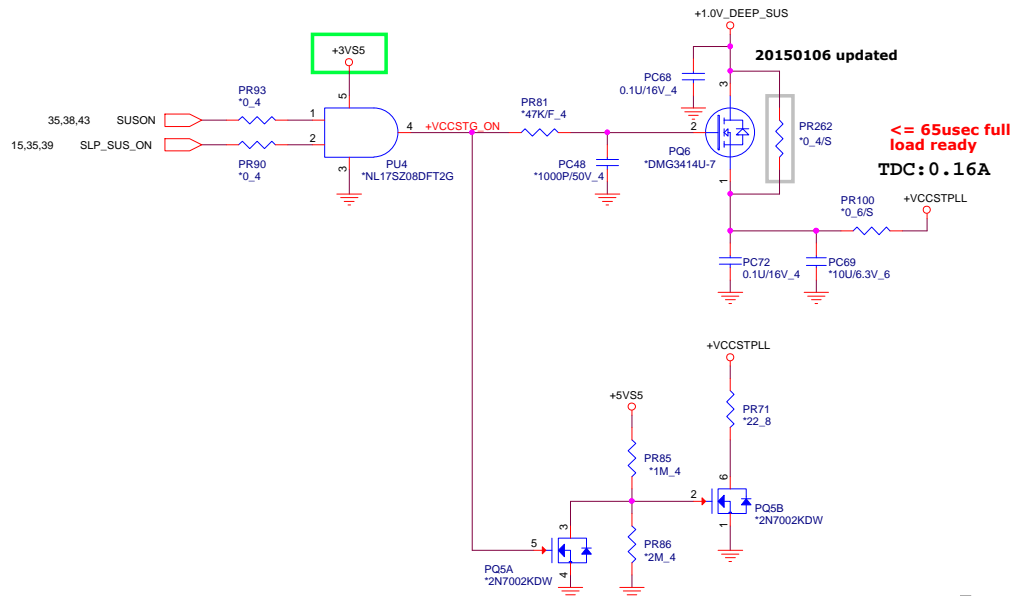
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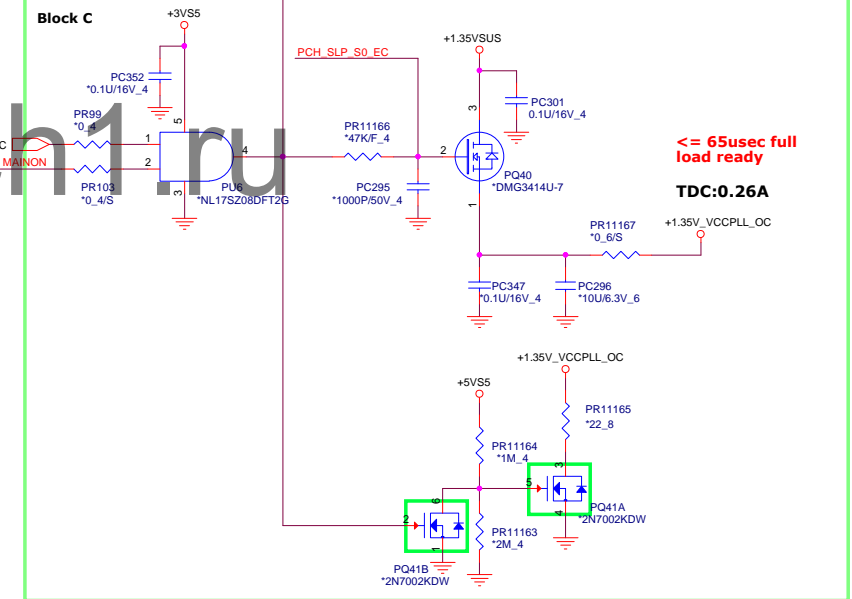




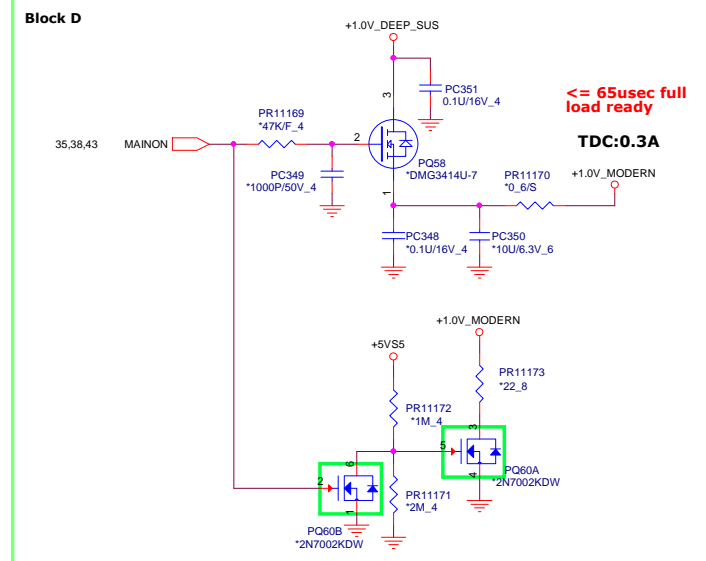
Support Modern standby mode

1. Remove Ra/Rc & stuff Rb/Rd
2. stuff block C & D

Reserve for Modern StandBy



Reserve for Modern StandBy

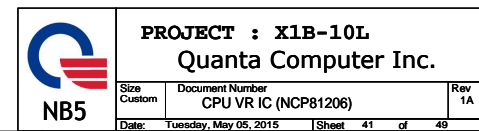


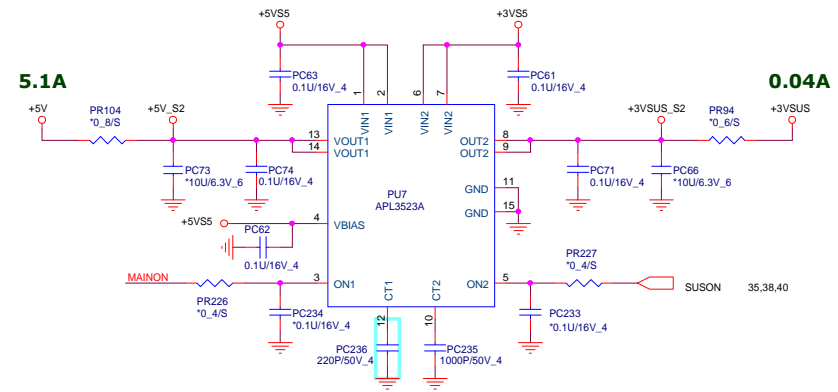
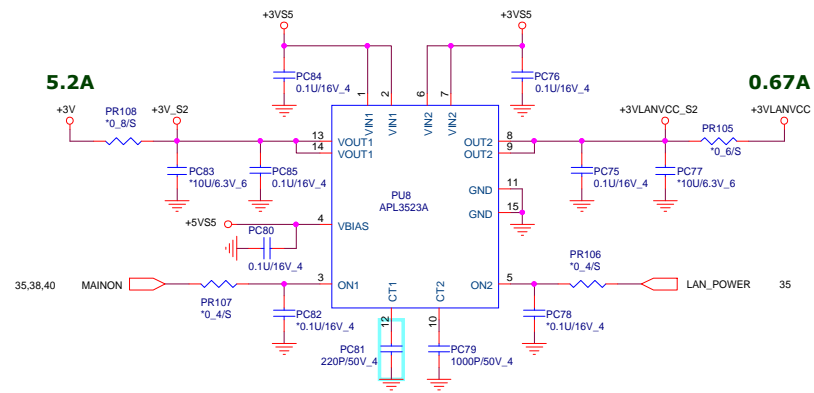
+1.0V	2,4,6,16,32,35
+3VS5	4,10,15,16,32,34,35,37,39,43,46
+5VS5	4,30,32,33,37,38,39,41,42,43,44,45,46
+VCCIO	2,6,16
+1.35VSUS	3,6,17,18,38,46
+VCCSTPLL	2,4,5,6,8,41
+1.0V_DEEP_SUS	9,13,15,16,39
+1.35V_VCCPLL_OC	6



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Quanta Computer Inc.

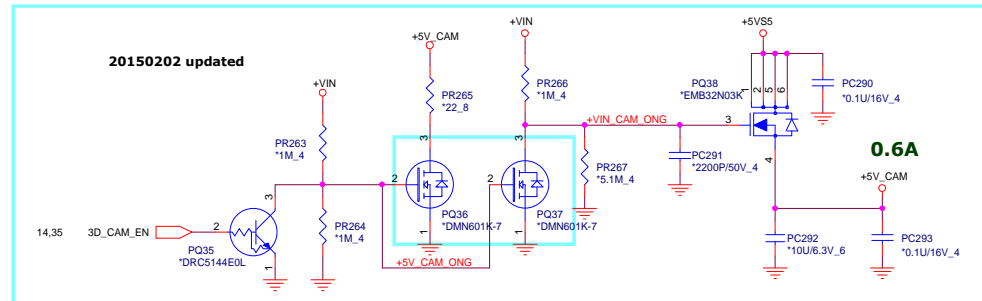
Size Custom	Document Number +1.0V/+VCCSTPLL	Rev 1A
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+3V	2, 4, 10, 11, 12, 13, 14, 15, 16, 17, 18, 20, 27, 28, 29, 30, 31, 32, 33, 34, 35, 41, 44
+5V	28, 29, 30, 31, 32, 33, 34
+VIN	28, 31, 33, 34, 36, 37, 38, 39, 41, 42, 44, 45, 46
+3VSS	4, 10, 15, 16, 32, 34, 35, 37, 39, 40, 46
+5VSS	4, 30, 32, 33, 37, 38, 39, 40, 41, 42, 44, 45, 46
+3VSSUS	31, 33
+5V_CAM	33
+3VLANVCC	30, 32

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For Acoustic

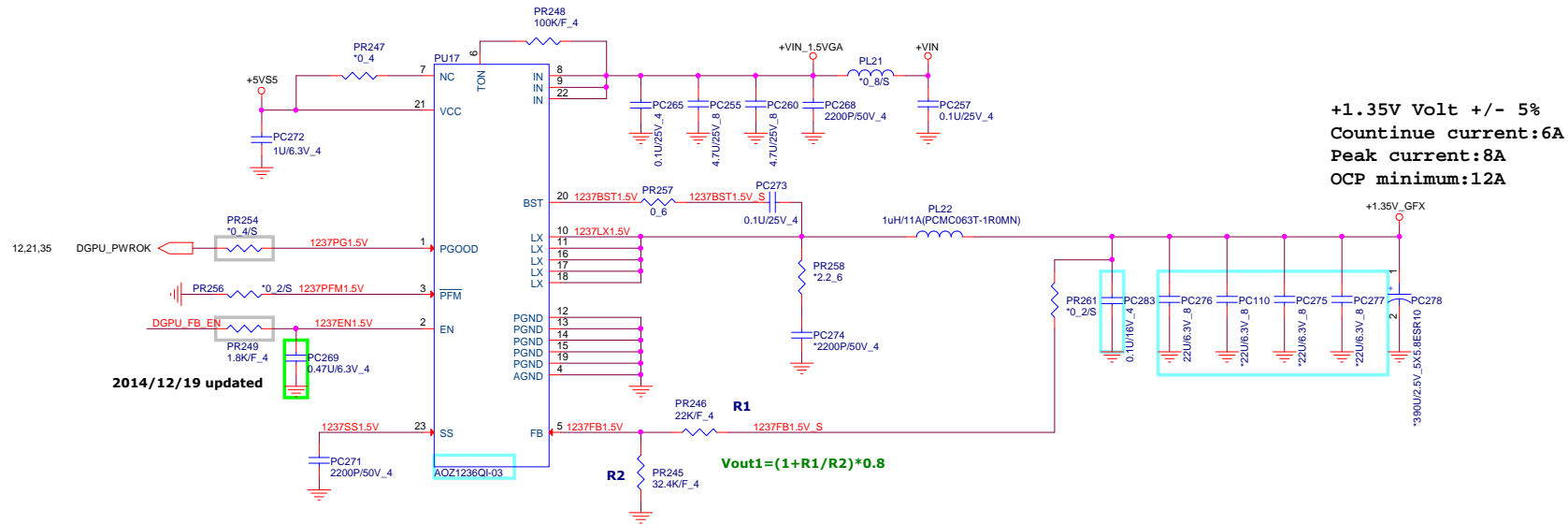
N16S-GT (23/18W)

EDP: 26A

EDP peak: 51A

OCP minimum 56A

+3V	2,4,10,11,12,13,14,15,16,17,18,20,27,28,29,30,31,32,33,34,35,41,43
+VIN	28,31,33,34,36,37,38,39,41,42,43,45,46
+5VS5	4,30,32,33,37,38,39,40,41,42,43,45,46
+3V_GFX	19,21,22,46
+VGCORE	19



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